Abstract

Metal-semiconductor (M-S) junctions are prepared in this study by thermal evaporation technique, in which we used indium (In), silver (Ag) and gold (Au) films and aluminum (Al) films.

The Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au diodes heat treated at different annealing temperatures 303,373 and 473 K. The ohmic contact was aluminum with thickness of about 0.2 µm and the Schottky contacts were indium, silver and gold with thickness of (0.1, 0.2) µm under vacuum conditions of about 10^{-5} mbar.

The effects of annealing temperatures and work functions have been studied by current-voltage and capacitance- voltage characteristics. The I-V characteristics showed that the rectification properties of all prepared diodes were improved with increasing the annealing temperature and the metal work functions (the ideality factor and the saturation current density decreased). The ideality factor (n), saturation current density (J_s) and the barrier height (Φ_B) were calculated using I-V plots with semilogarithmatic scale.

The current–voltage characteristic of Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au junctions showed that the current varies approximately exponentially with applied voltage and the junction was coinciding with recombination–tunneling model, the dark current decreases with increase of the thickness. Under illumination, the photocurrent increases and decreases with increase of annealing temperatures and thickness, respectively.

The C-V characteristics of Al/c-Si/In and Al/c-Si/Ag diodes have been prepared at different thickness except Al/c-Si/Au at thickness equal to 0.2µm and annealing temperatures. The reverse bias capacitance was measured as a function of bias voltage at frequency 1 MHz; the

capacitance decreases with increasing the reverse bias voltage, also with increasing of thickness and annealing temperatures.

The built-in voltage (V_{bi}), barrier height (Φ_B) and the carrier concentration (N_a) were calculated using Mott-Schottky plot (C^{-2} vs. V).

The d.c. conductivity measurements using Arrhenius plot ($\ln\sigma=f(10^3/T)$) showed that there are two activation energies E_{a1},$E_{a2.}$

The electrical activation energies increase with increasing annealing temperatures.

الخلاصه

تم في هدا البحث تحضير معدن - شبه موصل باستخدام تقنية التبخير الحراري بالفراغ،حيث استخدمنا اغشيه رقيقه من الانديوم و الفضه و الذهب و الالمنيوم ,*حيث تم معامله الثنائيات* Al/c-Si/In و Al/c-Si/Ag و Al/c-Si/Au حراريا بدرجات تلدين مختلفة (٣٠٣، ٣٧٣، ٤٧٣) كلفن . التوصيل الاومي لهذه الثنائيات كان من معدن الالمنيوم بسمك 0.2 مايكرومتر أما معادن اتصال شوتكي فقد كانت بسمك(٠,١، ٠,٢) مايكرومتر و ضغط تبخير بحدود ١٠$^{-٥}$ ملي بار.

تم في هذا البحث أيضا دراسة تأثير حرارة التلدين و تغيير دوال شغل المعادن على الخصائص التقويمية للثنائيات عن طريق دراسة خصائص تيار-جهد و متسعة- جهد لتلك الثنائيات، وقد لوحظ بان هناك تحسن بالخصائص التقويمية للثنائيات (انخفاض في عامل المثالية و في كثافة تيار الاشباع العكسي). واظهرت الدراسة ان كثافة تيار الأشباع (J_s) وحاجز الجهد (Φ_B) وعامل المثالية (n) تم حسابها بأستخدام خصائص تيار – جهد ذات المقياس اللوغارتمي لأحداثي التيار. بينت خواص تيار– فولتية للثنائيات Al/c-Si/In و Al/c-Si/Ag و Al/c-Si/Au بأن تيار الظلام الأمامي يتغير أسيا تقريبا مع فولتية الأنحياز و هذا يتفق مع نموذج أعادة الأتحاد – الأنتفاق و لوحظ نقصان تيار الظلام بزيادة السمك. ومن خلال قياسات تيار- فولتية تحت ظروف الأضاءة وجدنا أن التيار الضوئي يزداد مع زيادة درجة حرارة التلدين ويقل مع زيادة السمك .

درست خصائص السعة - الجهد للتراكيب الثنائية Al/c-Si/In و Al/c-Si/Ag ما عدا Al/c-Si/Au بسمك ٠,٢ مايكرو متر وبدرجات تلدين مختلفة. حيث قيست سعة الأنحياز العكسي كدالة لفولتية الأنحياز وبتردد ١ ميكاهيرتز وقد دلت هذه النتائج على ان السعة تقل بزيادة جهد الأنحياز العكسي، وبزيادة السمك ودرجات حرارة التلدين. قيم جهد البناء الداخلي (V_{bi}) ، حاجز الجهد (Φ_{Bp}) وتركيز الحاملات (N_a) تم حسابها بأستخدام علاقة شوتكي– موت [C^{-2} vs. V]. أظهرت قياسات التوصيلية المستمرة وبأستخدام علاقة آرهينوس[$\ln\sigma$ = f(10^3/T)] وجود طاقاتي تنشيط E_{a1} وE_{a2} والقيم المحسوبه تشير الى ان طاقات التنشيط تزداد بزيادة درجه حراره التلدين .

أظهرت قياسات التوصيلية المستمرة وبأستخدام علاقة آرهينوس[$\ln\sigma = f(10^3/T)$] وجود طاقاتي تنشيط E_{a1} و E_{a2} والقيم المحسوبه تشير الى ان طاقات التنشيط تزداد بزيادة درجه حراره التلدين .

Chapter One
General Introduction

1.1 Introduction

The rectifier effect in metal – semiconductor contact discovered by Braun in 1874, which forms the basis of one of the oldest semiconductor devices [1]. The device was used for a long time without thoroughly understanding. Wilson in 1931 , formulated the transport theory of semiconductors which was based on the band theory of solids [2]. This theory was applied to the metal – semiconductor contact. In 1938, Schottky suggested that the potential barrier could arise from stable space charge in the semiconductor alone without the presence of a chemical layer. Mott thought that the difference between the work function of metal and semiconductors resulted in the existing potential barrier at M-S interface, and the region of the barrier was deprived of charged impurities. In addition to the theories of Schottky and Mott, the thermionic emission theory, which is the process of emission of electron into metal causing the current, was introduced by Beth [1]. Schottky metal contacts show rectifying behaviors. Furthermore, the difference between experimental and predicted value of barrier heights, Bardeen proposed that the discrepancy might be due to the effects of surface states, which can pin the Fermi level in the center of the band gap. In the late 1940, industry has utilized the properties of electrical contact to realize semiconductor components such as high speed Schottky diodes [3].

Schottky rectifier has been used in the power supply industry. The primary advantages are very low forward voltage drop and switching speeds that approach zero time making them ideal for output stage of

switching power supplied. This latter feature has also stimulated their additional use in very low power involving signal and switching diode requirements of less than 100 Picoseconds [4].

The Schottky diode is widely used in the electronic industry because of the applications of these junctions in integrated circuit technology and for light detection and solar energy conversion purposes. Schottky diode is a unipolar device in which the current transport is mainly due to majority carrier compared to P- N diode although they have the similar I-V characteristics. Schottky diodes where selected because they are easy to fabricate, growth and study [4].

1.2 Schottky Barrier Devices

These devices as in Figure (1-1) made from deposition thin film from pure metal on semiconductor clear surface, that's called metal-semiconductor contact, it's unipolar charge of majority carrier that's dominant on contact operation which has only one kind of charges, by it we could get the rectifier character as a result of potential barrier that creates by finding stable space charges in semiconductor, this simple model built on this theory called Schottky barrier model.

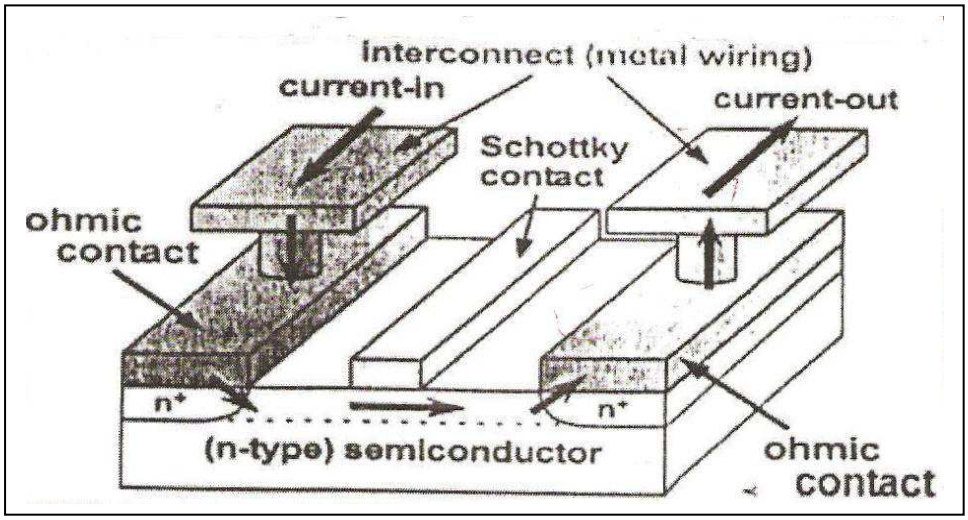


Fig. (1-1) Picture of Schottky barrier shown how the current getting in and getting out [4].

Figure (1-2a) shows semiconductor-metal before contact explain the imparity of Fermi level cause electrons inflow to semiconductor, while in Figure (1-2b) Schottky barrier that created after semiconductor-metal contact. The disproportionate space results void charges which cause slipping voltage in the interstitial surface.

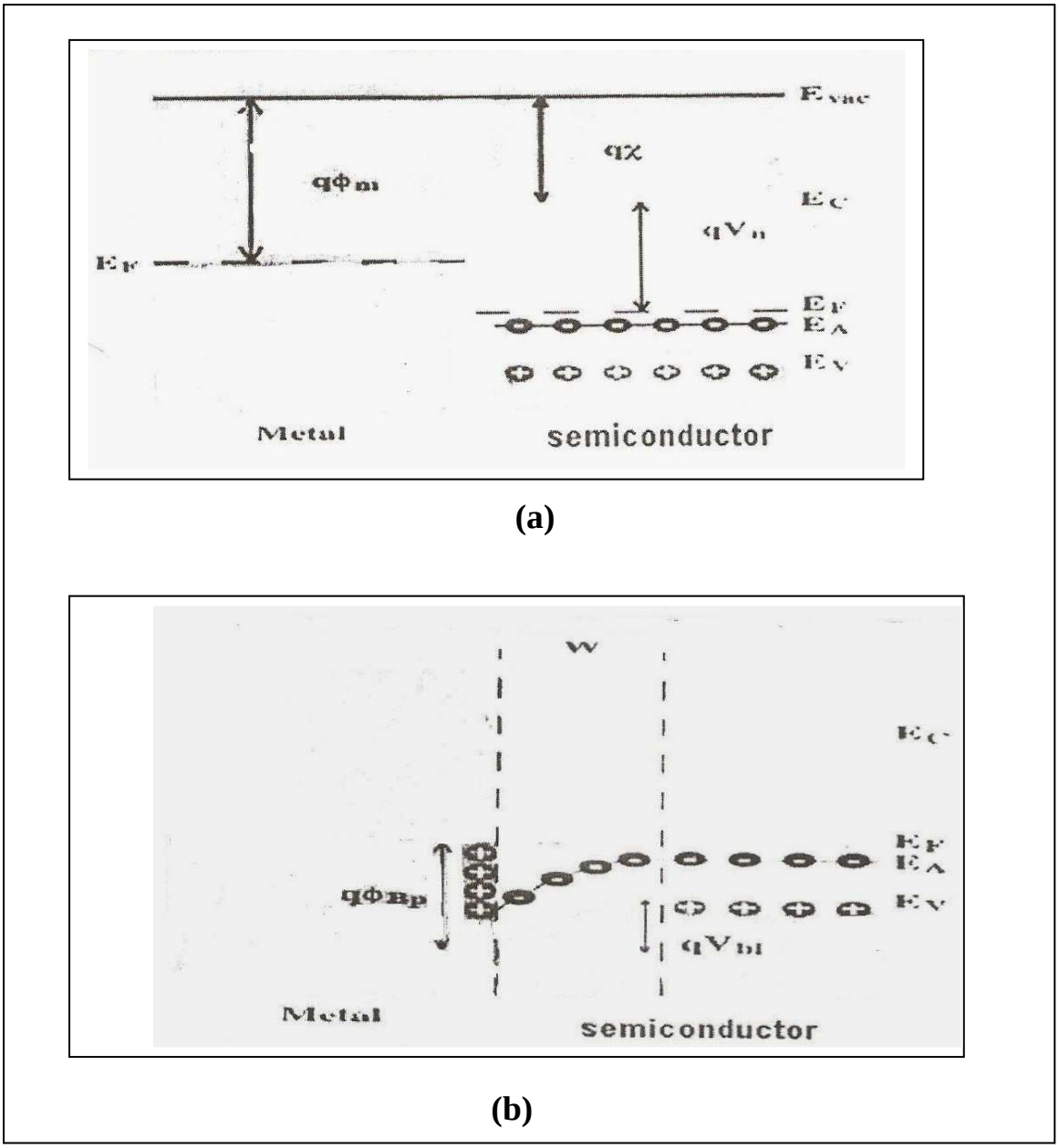


Fig. (1-2) Metal-semiconductor (a) Before creating Schottky barrier (b) After creating Schottky barrier [5]

1.3 Metals-Semiconductor Contacts

Figure (1-3a) shows the energy band diagram for n-type semiconductor and metal, the Fermi level for semiconductor will be upper the Fermi level for metal before contact.

Figure (1-3b) shows the n-type semiconductor-metal contact at the thermal equilibrium, where the used metal work function must be greater than the electron affinity for the semiconductor.

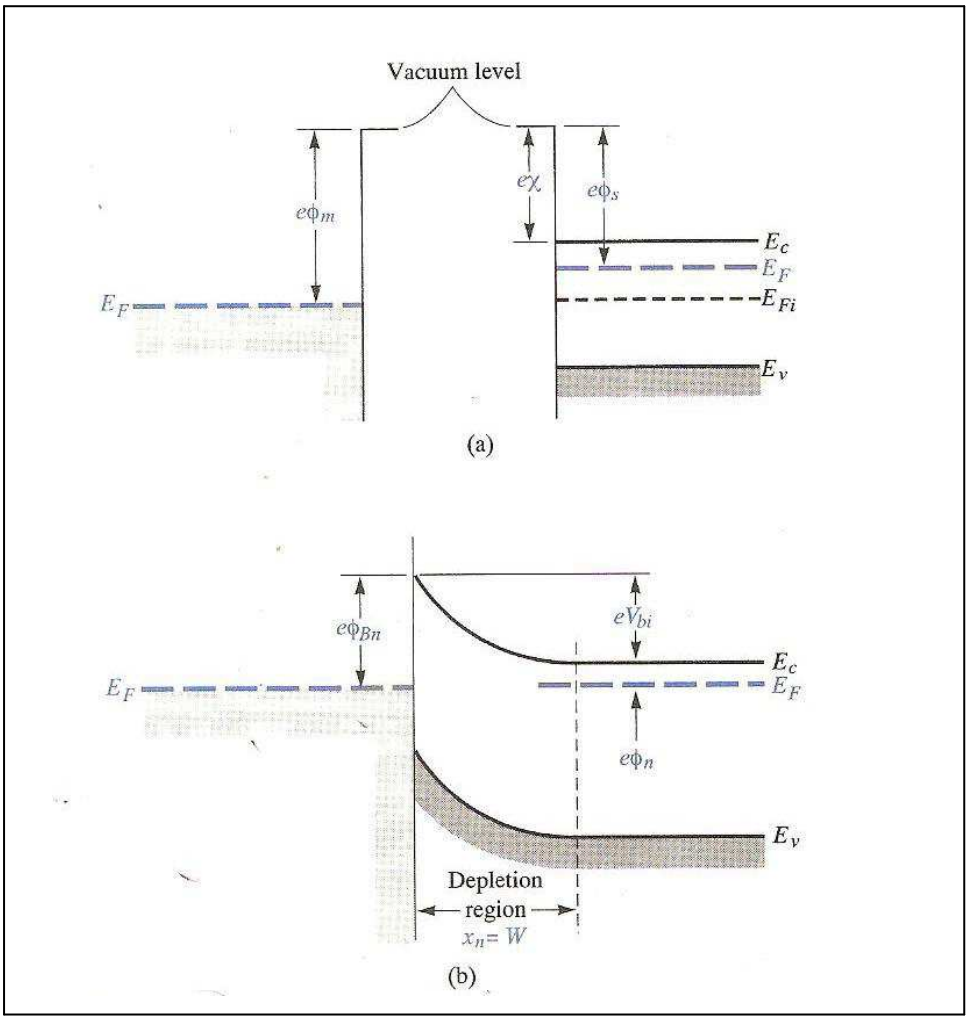


Fig.(1-3) Energy band diagram of metal- n-type semiconductor contact when $\phi_m > \chi_s$. (a) Before contact (b) After contact [6].

The barrier height Φ_{Bn} is determined by the difference between the metal work function ϕ_m and the semiconductor electron affinity χ_s

$$\phi_{Bn} = \phi_m - \chi_s \quad \text{..... (1-1)}$$

Where: -

χ_s: is the electron affinity of the semiconductor, defined as the energy difference between the bottom of the conduction band and the vacuum level.

ϕ_m : is the metal work function, defined as the energy difference between the Fermi level and vacuum level.

Figure (1-4a) shows the p-type semiconductor –metal before contact and Figure (1-4b) shows the p-type semiconductor- metal contact at the thermal equilibrium, where the used metal work function must be less than the electron affinity for the semiconductor. Before contact the upper end of valance band under Fermi level but at the contact it's will be under the positive about χ_s, so that the formed barrier for flowed electrons from metal to semiconductor and the flowed holes from p-type semiconductor to metal [6,7].

$$\phi_{Bp} = E_g - (\phi_m - \chi_s) \quad \text{..... (1-2)}$$

Where:

E_g : is the band gap of the semiconductor.

The barrier height is independent of the semiconductor doping concentration.

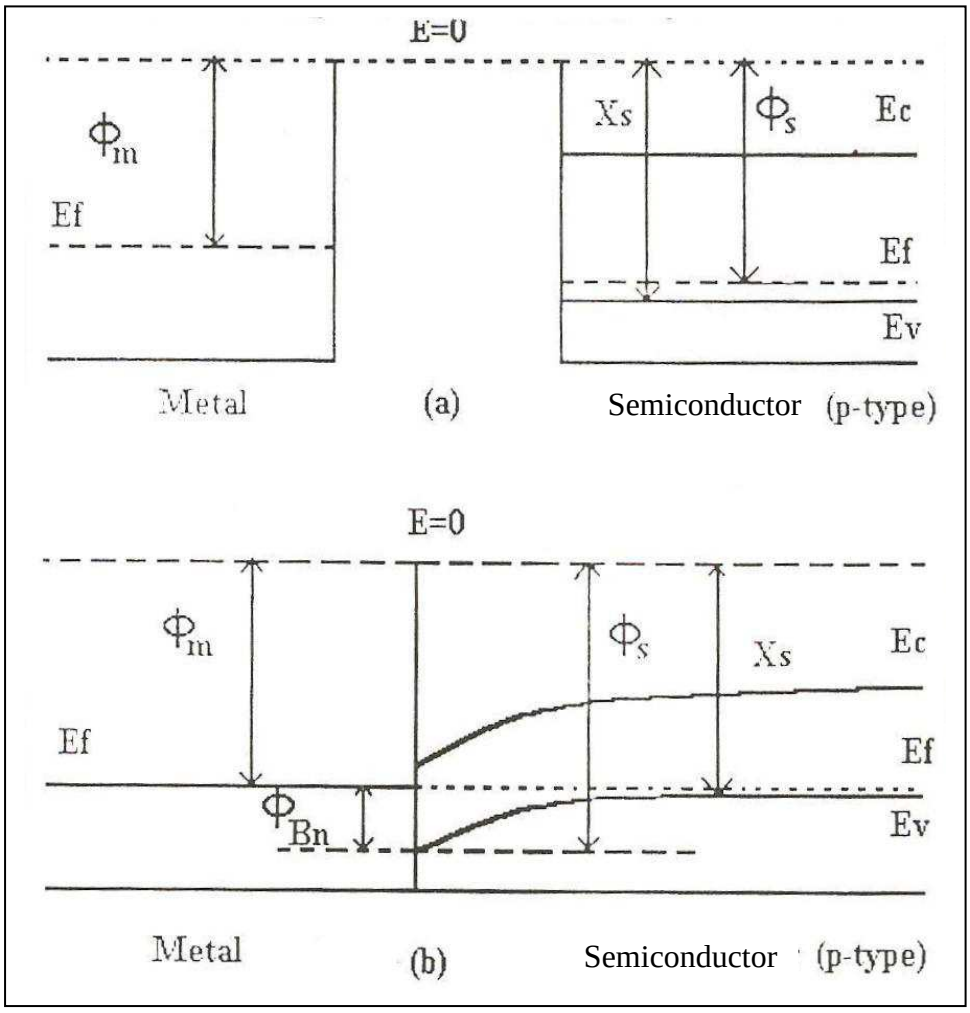


Fig.(1-4)Energy band diagram of metal- P-type semiconductor contact when $\phi_m < \chi_s$. (a) Before contact (b) After contact [6,7,8].

1.4 Effect Bias and Band Bending

When a negative voltage is applied on n-type semiconductor according to the metal, the electrons static energy of the conduction band in the depth of depletion region will increase and level will be move upward an energy equal (1eV).

The potential barrier to movement of electrons in semiconductor to the metal inward of contact will decrease which leading to increase the

passing current in the semiconductor to the metal, so that will be the depletion region negative to a small voltage leading to formation high current during contact, it's contact instate of forward bias [9].

When a positive voltage is applied on semiconductor according to the metal, so electrons passing barrier to the metal and semiconductor holes to crossing contact remain constant with bias, but metal holes barrier and semiconductor electrons will change (increase) because static energy of electrons of conductor band in the depth region will decrease, so Fermi level will move down with an energy equal (1eV).

The current of semiconductor and current of metal holes will decrease, since contact barrier is inversely bias and make the depletion region positive.

In the case making p-type semiconductor positive according to the metal (i.e. positive voltage is applied on the p-type semiconductor), this voltage will decrease barrier of majority carriers when region (p) positive (forward bias), since electrons current in metal will cross the barrier to semiconductor and holes of semiconductor will bass to the metal.

When a negative voltage is applied on p-type semiconductor according to the metal, this voltage will increase barrier of bass majority carriers through contact and it's inversely bias [9].

Band bending can occur just below free semiconductor surface, and when metals or oxides come into contact with semiconductors. The major effect is caused by the presence of surface states in the gap, which pins the Fermi level, and the Fermi level induces band bending.

As in Figure (1-5) for n-type semiconductor, the band bends upward towards the surface. This bending is associated with a dipole layer beneath the surface corresponding to the depletion region. For a p-type semiconductor, band bending is reversed and surface states are charged positively.

The change in the energy band diagram for metal-semiconductor contacts for both type semiconductors due to different biasing conditions as in Figure (1-5a). The built-in potential, V_{bi} , due to the different biasing condition for both n-type and p-type semiconductors [10].

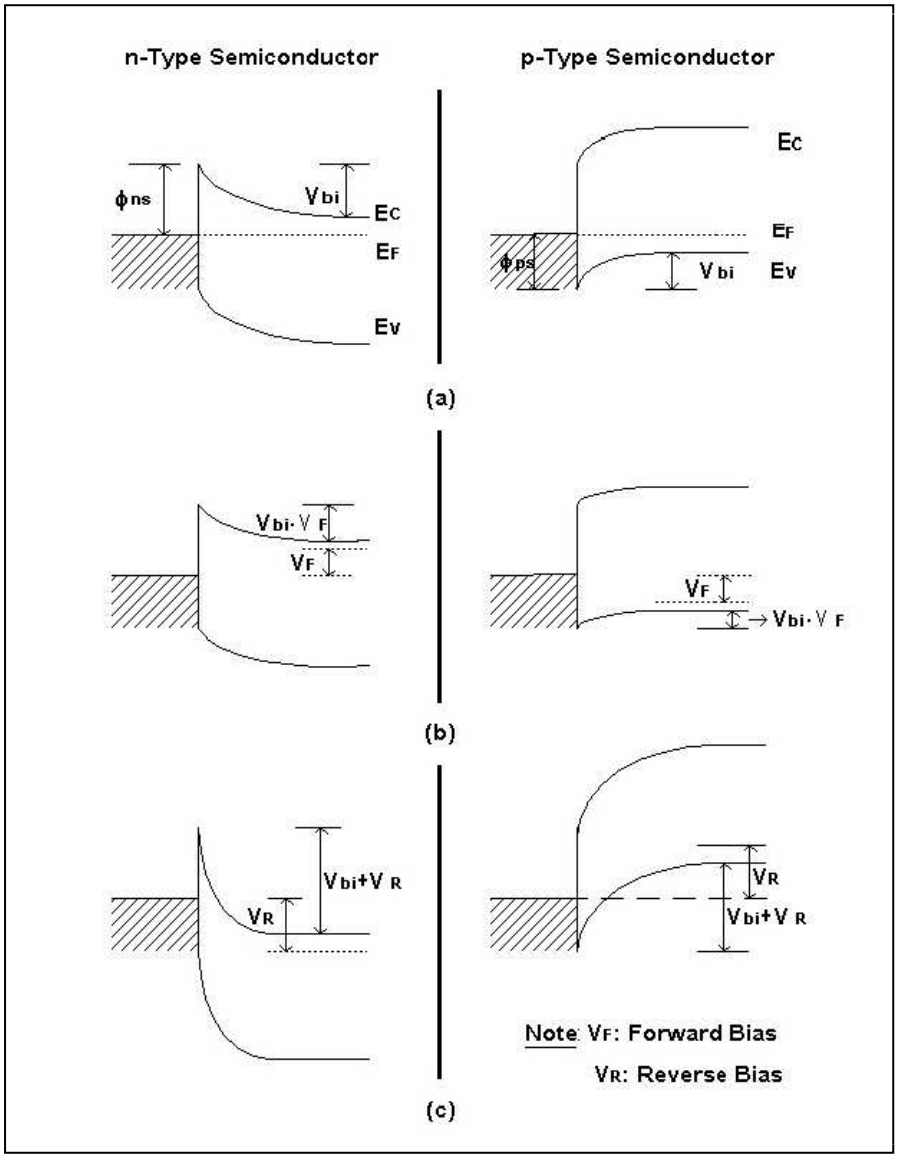


Fig.(1-5) Energy band diagram of metal n and p-type semiconductor under different biasing condition (a) Thermal equilibrium, (b) Forward bias, (c) Reverse bias [10].

The rectifying character of the contact is determined by the symmetry with respect to $\pm V$. Using forward-bias voltage (positive V) is applied to the Schottky barrier of Figure (1- 5b); there are many electrons with enough thermal energy to cross the barrier potential into the metal. As a result, the contact potential is reduced from V_{bi} to $V_{bi} - V_F$. When the Schottky diode is reverse biased, the potential barrier for electrons becomes large, hence there is a small probability that an electron will have sufficient thermal energy to cross the junction, a reverse bias increase the barrier to $V_{bi} + V_R$ as in Figure (1-5c) [5]. In the case of the metal/p-type semiconductor as in Figure (1-5b), forward current increase as the voltage lowers the potential barrier to $V_{bi} - V_F$ and holes flow from the semiconductor to metal. Of course, reverse voltage increases the barrier for hole flow and the current becomes negligible [10].

1.5 Current Transport Mechanism in Schottky Contact

The current transport in metal-semiconductor contact is mainly due to majority carriers. Figure (1-6) shows four basic transport processes at a metal/semiconductor interface under forward bias. The inverse processes occur under reverse bias [11].

The processes are:

1.5.1 Thermionic Emission

Transport of electrons from the semiconductor over the potential barrier into the metal, which is the dominant process for Schottky diode with moderately doped semiconductors operated at moderate temperature.

1.5.2Tunneling (Field Emission and Thermionic Field Emission)

The other important process in metal – semiconductor current transport is tunneling. Just like metal – vacuum tunneling, in a metal-semiconductor interface, electrons may tunnel through the Schottky barrier without reaching the top of the barrier when the barrier width is not thick. Tunneling of electron through the barrier can contribute to the current either by direct tunneling of electrons from the Fermi level of the semiconductor to the metal (field emission) or with the assistance of thermal energy such that electrons will be excited to higher energy and tunnel through less the triangular barrier (thermionic field emission)[11].

1.5.3 Recombination in the Depletion Region

Yu and Snow studied the importance of injection of majority carriers in charge space region in semiconductor, and explain that under forward bias, and then the holes in metal will be injection in the depletion region of semiconductor, while the electrons will be injection inside neutral semiconductor.

This increment in couples (electron-hole) will be recombining in the depletion region to give forward recombination current. The recombination current will be a famous reason in the deflection from ideal behavior of Schottky diodes, and its importance will be concentrate in diodes that have higher barrier heights, less forward bias and lower temperature [12].

1.5.4 Hole Injections

In some cases at forward bias, some holes diffuse through neutral region of semiconductor and will cause the hole injection from metal to the inside of semiconductor, this process will happens when Schottky barrier height greater than half the hole band.

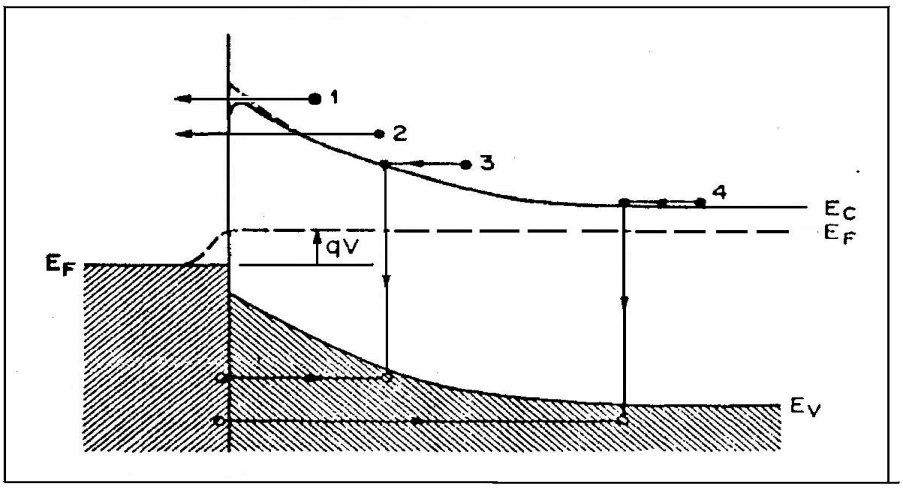


Fig. (1-6) Current transport mechanism in Schottky junction [11]

1.6 The Effects on Schottky Barrier

1.6.1 The Oxide Layer

In most metal-semiconductors, we can't reach to the ideal case. Because of a thin layer of oxide (1-2)nm which covers the semiconductor surface and called the interfacial layer as in Figure (1-7) [3,11].

This layer cause an additional barrier which result to increase the barrier height ϕ_B, and this new barrier is very narrow whereas the electrons can tunnel through it very easy [3,10].

The semiconductor surface contains surface states due to incomplete covalent bonds, which can lead to charges at the metal semiconductor interface. Furthermore the contact is seldom an atomically sharp continuity between the semiconductor crystal and the metal [3].

The contact potential which result from Schottky barrier potential and insulator layer potential called the effective barrier height ϕ_B.

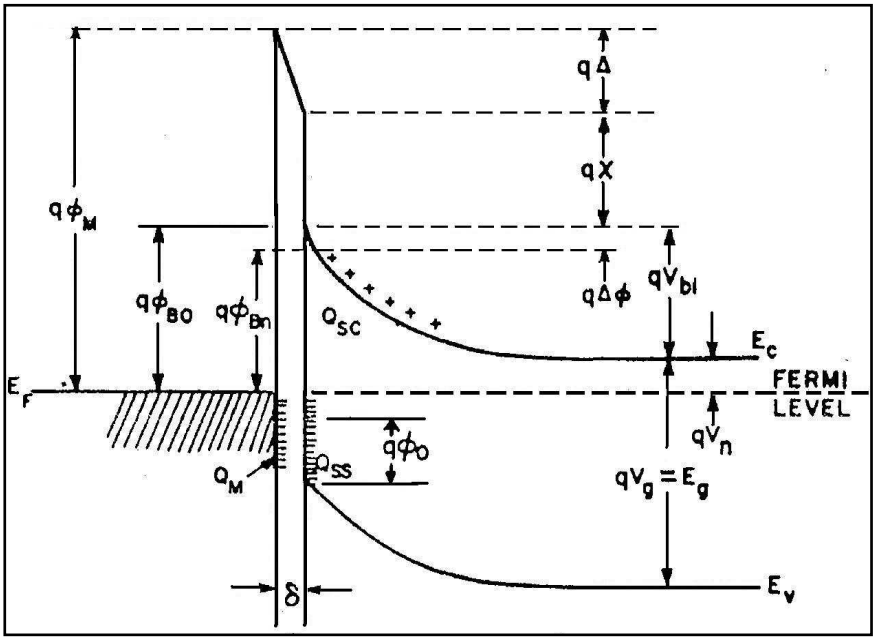


Fig. (1-7) Metal/ Semiconductor contact with interfacial layer [11]

1.6.2 The Surface States

The surface of semiconductors has a very high sensitivity to reaction with environment because of the non saturated bonds which obtainable in it. All these bonds act as acceptors like behaviors of electrons, then a negative layer generated on the surface of semiconductor, while a positive space charge generated inside the semiconductor. Then the energy bands will curve upward in respect of Fermi level [10].

The origin of the surface states comes from the discontinuity in the lattice or foreign atoms, or the oxide layer on the surface of the semiconductor. And the effect of the surface states is screening the semiconductor from the metal by generating an additional barrier between them. Also it absorbs the difference of potential contact between the semiconductor and metal [10].

1.6.3 Image Potential

The image potential is a fundamental phenomenon that can be changed in magnitude of the barrier height but no eliminated. It's the result of the attractive force experienced by charge carrier in vicinity of a metal surface due to an "Image force" of opposite sign induced in the metal. This attractive force is given by:

$$F_X = \frac{-q^2}{16\pi\varepsilon_S X^2} \qquad \ldots\ldots. (1\text{-}3)$$

Where

$F_{x:}$ is the image force

ε_s :is the permittivity of semiconductor

X :is the distance between the charge and the it's image

The image force increases with increasing doping level and decreases with increasing forward bias, as shown in Figure (1-8).

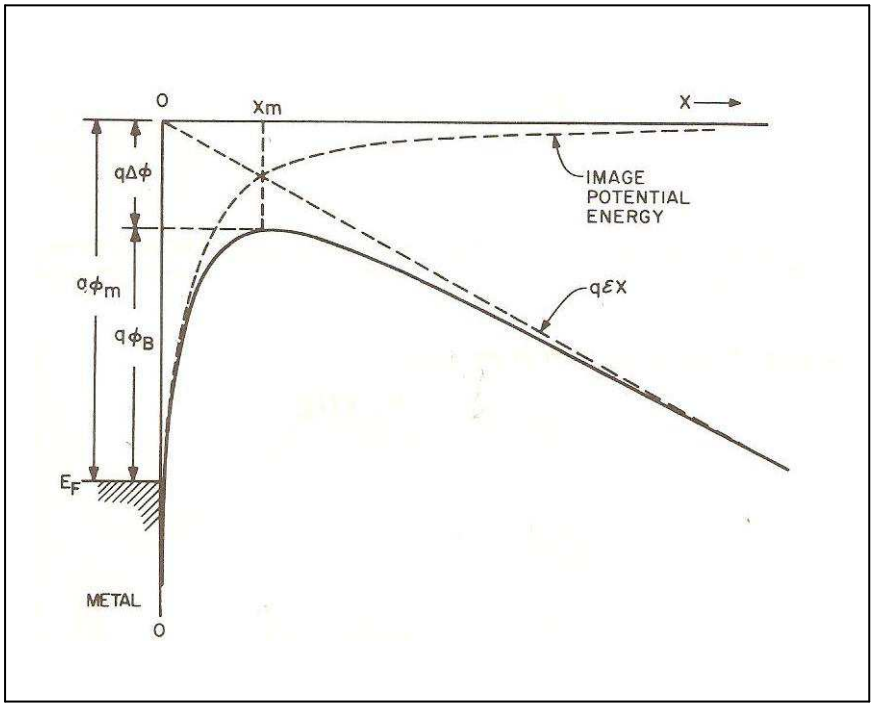


Fig. (1-8) Image force lowering of barrier [11]

1.7 Measurement of Barrier Height

1.7.1 Current – Voltage Measurement

In Schottky barrier diode made on high mobility semiconductor such as Si and GaAs, the current is due to the thermoionic emission of electrons over the barrier. The current flow mechanisms noted above were first suggested by Beth and further defined by Crowell and Sze [11,13].

This current is written as follows

$$I(V) = I_s e^{\frac{qV}{nk_B T}}\left[1 - e^{\frac{qV}{K_B T}}\right] \quad \ldots\ldots\ldots\ldots (1\text{-}4)$$

Where,

q: is the electron charge

k_B : is Boatzman constant

T: is the absolute temperature is the applied bias

n: is the ideality factor.

I_s : is the saturation current, is given by

$$I_s = AA\exp\left[\frac{-q\Phi_B}{K_B T}\right] \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1\text{-}5)$$

Where

A*: is the Richardson constant,

A: is the area of the diode

ϕ_B : Schottky barrier height (SBH) of the junction.

This expression will be used to determine the SBH and ideality factor for the structures studied here. The measured forward(lnI –V) curve is plotted on semi - logarithmic plot. The linear region is fit to obtain the

slope and the Y-intercept. The ideality factor and SBH are found from the slope of the linear region and the saturation current, respectively, i.e.

$$\frac{1}{n} = \frac{k_B T}{q} \frac{d\left(\ln I_s\right)}{dV} \qquad \text{..... (1-6)}$$

$$\phi_B = \frac{k_B T}{q} \ln\left[\frac{A^* A T^2}{I_s}\right] \qquad \text{..... (1-7)}$$

1.7.2 Capacitance – Voltage Measurement

The barrier height can also be determined by the capacitance meurement. When a small ac voltage is superimposed upon a dc bias, charge of one sign are induced on the metal surface and charges of the opposite sign in the semiconductor [14]. In this time method the diode capacitance is measure as a function of applied reverse bias. The capacitance of Schottky diode in depletion region can be expressed as

$$\frac{1}{C^2} = \frac{2\left(V_{bi} + V\right)}{A^2 \varepsilon_s q N_a} \qquad \text{..... (1-8)}$$

Where

: is the built-in potential V_{bi}

: is the dielectric constant of semiconductor ε_s

: is the doping concentration N_a

The barrier height can be determined by by means of V_{bi} as,

$$\phi_B = V_{bi} + V_n + \frac{k_B T}{q} \qquad \text{..... (1-9)}$$

$$V_n = k_B T \ln\left(\frac{N_V}{N_a}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1\text{-}10)$$

Where:

$V_{b\,i}$: is the voltage intercept

V_n: the depth of the Fermi level below the conduction band, which can be compute if the doping concentration is known.

1.8 Ohmic Contact

This contact is also between metal and semiconductor. If, Φ_B, is zero or negative and electron can flow freely the contact. An ohmic contact is non rectifying contact, the current-voltage characteristic of the contact should be obey ohms law V=IR [15].

There are three mechanisms governing the transportation of current a across contacts. The first mechanism is known as thermionic emission (TE), where by carriers surmount the potential barrier. The dominant current transport mechanism for semiconductor with low doping level, $N_d < 10^{17} cm^{-3}$. As shown in Figure (1-9a). Second mechanism is known as Thermonic-Field Emission (TFE), which is applicable for semiconductors with intermediate doping levels, $10^{17} < N_D < 10^{19} cm^{-3}$. Thermionic Field Emission dominates Figure (1-9b). Field Emission or Tunneling (FE) is the third mechanism, which consists of carrier tunneling through the potential barrier. This mechanism is dominated when $N_D > 10^{19}$. As shown in Figure (1-9c). For in ohmic contact, the potential drop a cross the contact is directly proportional to the contact resistance, R_c , the specific contact resistance is defined by [16,17].

$$R_c = \left(\frac{dJ}{dV} \right)^{-1}_{V=0} \qquad \text{..... (1-11)}$$

For metal-semiconductor contacts with low doping, the current is governed by thermionic emission over the potential barrier.

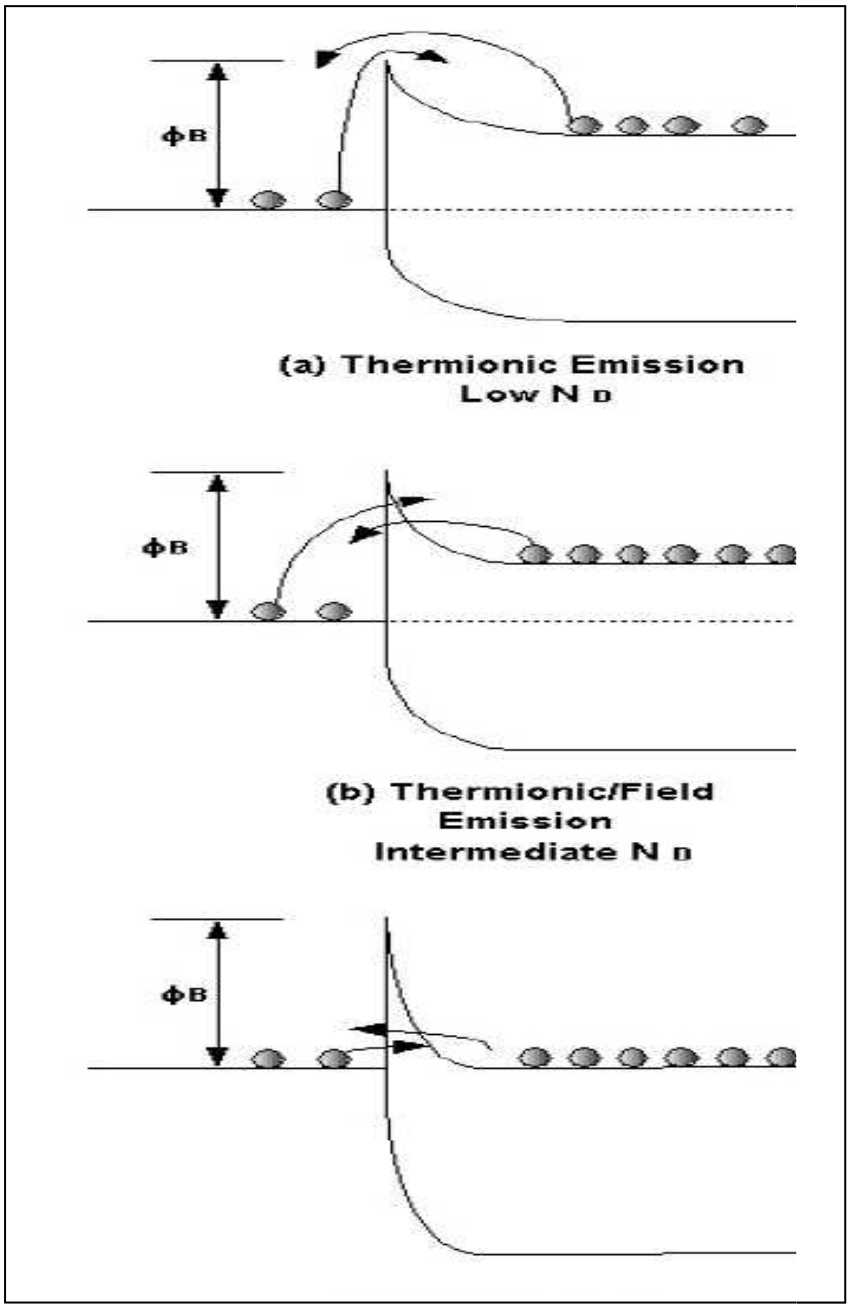


Fig.(1-9) Ohmic contact mechanisms: (a) Thermonic Emission(TE) (b) Thermonic Field Emission (TFE) and (c) Field Emission (FE) [17].

1.9 Literature Survey

The metal/Si device is a useful device for optoelectronic devices solar cells and light emitting diodes (LED). Because of that many studies have been devoted to improve the performance of this device.

Seneschal and Basinski in 1968 [18] have made dark capacitance measurement on Au/Si Schottky barrier. This measurement was done below 235 K and above room temperature with carriers concentration 2×10^{12} - 4×10^{16} cm^{-3}, they found that the capacitance is lower at lower temperatures. The barrier height was between 0.66 – 0.95 eV.

Sze et al. in 1971 [19] studied the I-V characteristics of MSM structure that were based on the thermionic emission theory. When a uniformly doped semiconductor is thin enough that it can be completely depleted before avalanche breakdown occurs. In their study, they prepared MSM structures (PtSi–Si–PtSi) of n-type silicon with doping 4×10^{14} cm^{-3} and thickness of 12 μm.

Gutkin and Sedov in 1975 [20] have fabricated Au/n-Si Schottky barrier with carriers concentrations of 10^{13} to 10^{17} cm^{-3} in the base illuminated with photons energy up to 5.2 eV. They studied the optical properties of the barrier of silicon single crystal grown by epitaxial growth. The rectifying contacts were formed by thermal evaporation in vacuum.

In 1989, Fang and Yang [21] describe the observation of aluminum diffusion into the silicon base of Al/W/Si ohmic contacts during aluminum annealing, and its effect on the ohmic property of the contact. The contacts were examined by specific contact resistance measurement, I/V characteristic measurement.

In 1995, Turut *et al* [22] presents an attempt related to the charging behaviour of interface states to the nonideal forward bias current-voltage (I-V) and the reverse bias capacitance-voltage (C-V) characteristics of

Al-nSi Schottky barrier diodes. The diode showed nonideal I-V behaviour with an ideality factor of 1.50 and was thought to have a metal-interface layer-semiconductor configuration. Considering that the interface states localized at the interfacial layer-semiconductor interface are in equilibrium with the semiconductor.

In 1997, Racko *et al* [23] indicated that the contribution presents a thermionic emission-tunnelling theory of the charge transport through a Schottky contact, valid for low injection. The approach extends the classical thermionic emission theory by incorporating the mechanism of tunnelling across the Schottky barrier.

In1998, Schmitz *et al* [24] indicated that the Contacts consisting of various single layer metals to n-type GaN had been formed and characterized. The current-voltage characteristics were measured for 17 different metals (Sc, Hf, Zr, Ag, Al, V, Nb, Ti, Cr, W, Mo, Cu, Co, Au, Pd, Ni, and Pt) deposited on the same epitaxial growth layer. The barrier height, ideality factor, breakdown voltage, and effective Richardson coefficients were measured from those metals which exhibited strong rectifying behavior. The barrier heights for these metal contacts were measured using current-voltage-temperature and capacitance-voltage techniques. It was found that an increase in metal work function correlated with an increase in the barrier height. In general, the SBH of various metals are influenced by the metal work function and also by the semiconductor surface preparation

In 2001, Lee *et al* [25] investigated Schottky barrier diodes of several metals (Ti, Ni, and Au) having different metal work functions to p-type Si (001) using I–V and C–V characteristics. Contacts showed excellent Schottky behavior with stable ideality factors of 1.07, 1.23, and 1.06 for Ti, Ni, and Au, respectively, in the range of 24°C to 300°C. The

measured Schottky barrier height (SBH) was 1.96, 1.41, and 1.42 eV for Ti, Ni, and Au, respectively, in the same temperature range from I–V characteristics. Based on their measurements for p-type Si, the SBH (Φ_{Bp}) and metal work functions (Φ_m) showed a linear relationship of $\Phi_{Bp} = 4.58 - 0.61\Phi_m$ and $\Phi_{Bp} = 4.42 - 0.54\ \Phi_m$ for I–V and C–V characteristics at room temperature, respectively. They observed that the SBH strongly depends on the metal work function with a slope (S ≡ φBp/φm) of 0.58 even though the Fermi level is partially pinned. They found the sum of the SBH ($\Phi_{Bp} + \Phi_{Bn} = E_g$) at room temperature for n-and p-type 4H−SiC to be 3.07 eV, 3.12 eV, and 3.21 eV for Ti, Ni, and Au, respectively, using I–V and C–V measurements, which are in reasonable accord with the Schottky-Mott limit.

In 2005, Zaggout and El-Gomati [26] state that the effect of heat treatment on the electrical behavior of aluminum on n-type silicon (Al/Si Schottky junctions) is used to study the effect of barrier height variation on secondary electron dopant contrast by annealing to 500°C. In this study, the variation of the Schottky barrier height had been detected as an increase of the contrast between Al on p+ and Al on n-type Si doped regions. This increase is attributed to a decrease the ideality factor of the Al/n-type Si contact due to an increase in the Schottky barrier height after annealing.

Karatas *et al* [27] had performed behavior of the non-ideal forward bias current–voltage (I–V) and the reverse bias capacitance–voltage (C-V) characteristics of Zn/p-Si (metal–semiconductor) Schottky barrier diode (SBDs) with thin interfacial insulator layer. The forward bias I–V and reverse bias C–V characteristics of SBDs have been studied at the temperatures range of 300–400 K. SBD parameters such as ideality factor

(n) determined Cheung's functions and Schottky barrier height, Φ_B were investigated as functions of temperature.

Okutan *et al* [28] investigated the electronic and interface state distribution properties of Ag/p-Si Schottky diode and showed that the diode indicates non-ideal current–voltage behavior with an ideality factor greater than unity, and the capacitance–voltage (C–V) characteristic is linear in reverse bias indicating rectification behavior and charge density within depletion layer is uniform, and found that From I–V and C–V characteristics, junction parameters such as diode ideality factor and barrier height were found as 1.66 and $\Phi_{B(I-V)}$ = 0.84 eV ,$\Phi_{B(C-V)}$= 0.90 eV respectively.

In 2006, Gould [29] said that the dependence of electrical conductivity (or resistivity) and the temperature coefficient of resistivity in thin films has been discussed, in particular the models of Thomson.

In the same year Stamov and Tkachenko [30] established that the space-charge region at the metal-semiconductor interface represents in fact a Schottky layer formed owing to a high concentration of deep-level centers. The charge transport in the conducting direction for these structures is related to the above-barrier emission of electrons and is consistent with the diffusion theory for one or two types of charge carriers. The high concentration of ionized centers in the space-charge region gives rise to the tunneling mechanism of breakdown in the blocking direction.

In 2007, Altindal *et al* [31] said that the Al/p-Si Schottky diodes with the native interfacial insulator layer (SiO2) were fabricated on the same quarter Si wafer. The Schottky barrier height (SBH), ideality factor

(n), these diodes had been calculated from their experimental forward bias current–voltage (I–V), reverses bias capacitance–voltage (C–V) measurements. Even though they are identically performed on the same quarter Si wafer, the calculated values of SBH have ranged from 0.680 to 0.736 eV, and ideality factor n from 1.62 to 2.87. It was found that the values of barrier height obtained from C–V characteristics are larger than that of the value from I–V characteristics.

1.10 The Aim of The Research

The essential aim of this work was to fabricate Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au junction using thermal evaporation methods and then to study the effect of thickness, annealing temperature and different Schottky electrodes on electrical properties of Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au for comparing the results with the previous study. Also study the dependence of saturation current density (J_s), ideality factor (n) and barrier height Φ_B on preparation condition with different metal work functions.

Chapter Two
Experimental Work

2.1 Introduction

This chapter describes the technique which is employed to produced (M-S) Schottky diode and include the measurement of the electrical properties of c-Si as well as the measurement of Schottky barrier diodes.

In the beginning we examined the evaporate the ohmic contacts and Schottky electrodes by thermal evaporation, and then annealed the film at the different annealing temperatures to investigate the electrical properties of these films. Electrical measurements were made for those junctions which include current-voltage characteristics, capacitance – voltage characteristics and D.C. conductivity. Ideality factor was determined from I-V measurements, barrier height and saturation current density. Built-in potential and carrier concentration were calculated from C-V measurements.

The scheme of experimental work is shown in Fig. (2-1).

2.2 Silicon Wafer Substrate

Single crystal silicon wafer was cleaned using etching processes that are summarized as follows:

1- Emerged the silicon wafer in diluted HF (1:10) concentration for 10 min.

2-Then immersed in distilled water for several times with ultrasonic vibration

3- Finally, they are dried by using air blower and wiped with soft paper.

2.3 Masks Preparation

The mask was a piece of thick aluminum foil. Shape of mask was used on substrate to evaporate suitable shape of electrodes, different type of masks used in Schottky diodes for ohmic contact and Schottky electrodes for I-V and C-V measurement as shown in Figure (2-2).

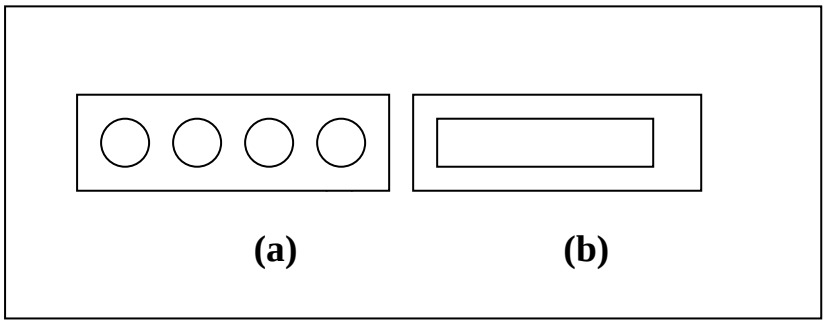


Fig. (2-2) Shape of some masks

(a) Mask use in Schottky electrodes (b) mask use in ohmic contact

The mask was cleaned using the following stages:

1 - The mask is rinsed in HCl (5%) for 5 min.

2- Then it is washed in distilled water.

3- It has immersed in a pure alcohol for 10 min.

4- It is dried by heating in furnace at 373 K for 10 min.

2.4 The Specification of Boat

The evaporation method requires using a boat or filament of tungsten, tantalum or molybdenum as sample evaporation source; the suitable boat must posses high melting point and should not react with the evaporated material. The design and shape of the boat must also be selected. To evaporate the aluminum electrodes a basket or spiral filament of tungsten (W) of (3683 K) melting point was used. A molybdenum boat (T_a) of (2895 K) melting point was used to evaporate (In, Ag and Au), as shown in Figure (2-3).

The current was passed through the boat in order to clean it and drive off the surface contamination. The temperature that was produced from the current should be below the melting point of the boat material.

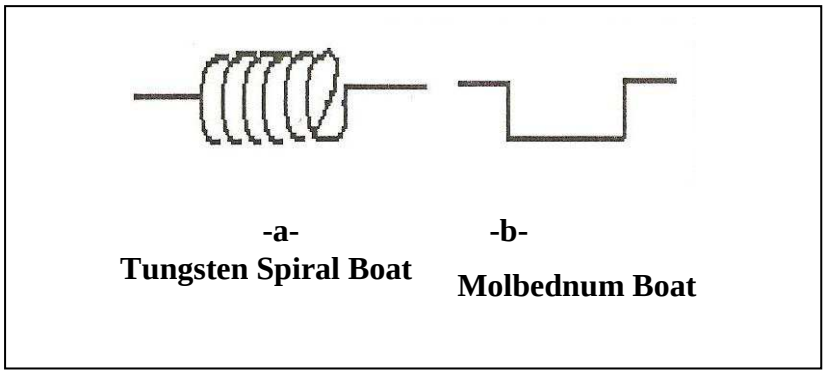


Fig.(2-3) Boats that be used in the fabrication steps.

2.5 Annealing Process

Annealing means exposed the sample or the thin film to a certain temperature for a certain time. Annealing in almost time its work with certain gas or air.

It helps to decrease the crystal defects by giving a kinetic energy to the atoms of the material, so that an atoms rearrangement will take place in the crystal structure.

Annealing for thin films cause sometimes decreasing in the resistivity of film because of forming a new state levels inside the energy band and that will make the resistivity decreased or its may be caused increased the resistivity in the film as result of removed the state levels inside the energy gap.

2.6 Thermal Evaporation in Vacuum

Thermal evaporation in vacuum represents the oldest and the most effective way that used to deposition thin films, where the formation of the film is contained the following steps: -

1- By using evaporation the deposition material will be in the gas state
2- Remove the atoms from the evaporation source to the substrate by help of vacuum
3- Deposition average of the materials on the substrate

The evaporation happened through putting material in a boat of Mo or W, and by using the right boat depending on the quality of the material that wanted to be deposit and after that the boat will be heated by passing an electrical current until the evaporated temperature of the material to be deposited on the substrate

Preparation of thin films in this way depends on the following steps:-

1- The space in the preparation room
2- The quality of the contained material of the preparation room
3- The displacement between the material and the substrate that evaporated on it
4- The temperture of the substrate
5- The average of the deposition
6- The from and kind of the boat
7- Thickness of the semiconductor

2.7 Coating Unit System

The vacuum unit system, which is used to prepare thermally evaporated Al\ c-Si \M was Edward coating unit model 306A. The vacuum consist of three main important parts, the vacuum enclosure (champer), the rotary pump which represents the first stage of vacuum technique called roughing stage and would provide the pressure in the chamber to about 10^{-2} mbar, while the diffusion pump which represents the second stage, called the high vacuum stage by which the pressure decreases to about 4×10^{-5} mbar. The main construction of the vacuum unit is shown in Figure (2-4).

The substrates were fixed on a spherical holder and placed in position at height of about 15 cm above the boat.

When the system is diffusion pumped down to a vacuum of 10^{-5} mbar, an electric current was passed through the boat gradually to prevent breaking the boat, when the boat temperature reached the required temperature the deposition process starts with constant deposition rate. After these steps the current supply was switched off and the samples were left in the high vacuum for one day; and then the air was admitted to the camper, and the films were taken out from the coating unit and kept in the vacuum desiccators until the measurements were made.

All the samples were prepared under constant conditions (pressure, substrate temperature and rate of deposition); the main parameters that control the nature of the film properties are thickness (0.1, 0.2) µm and annealing temperature (373 and 473) K

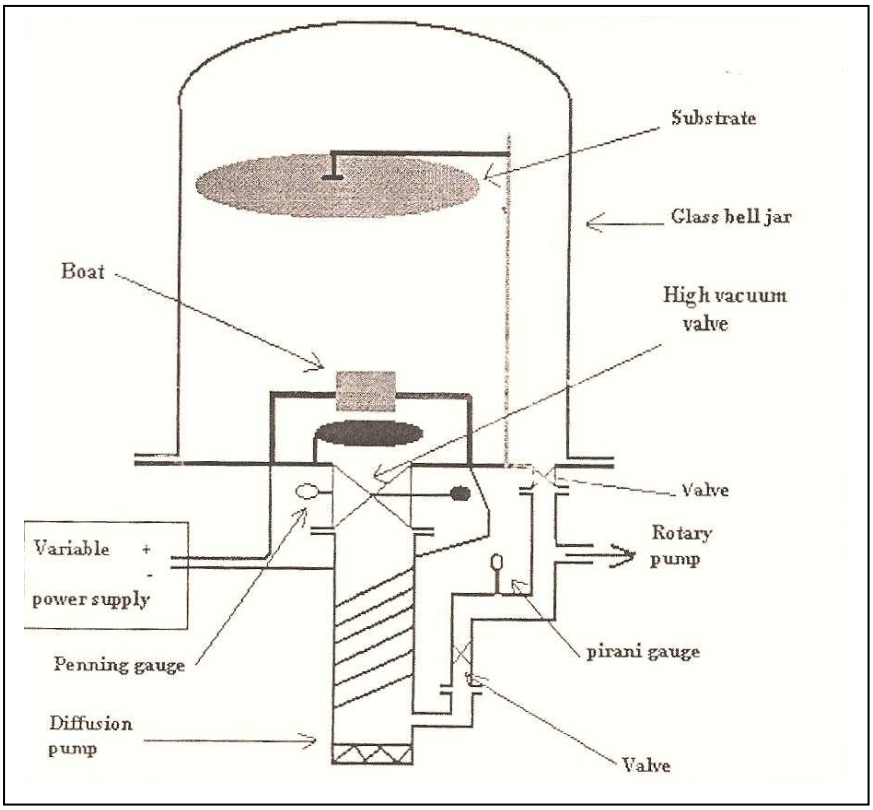


Fig. (2-4) Typical coating system[32].

2.8 Ohmic Contacts

Ohmic contact for silicon and fabricated devices were produced by thermal evaporation technique. The Edward E306A coating system was used for this purpose, under low pressure of 10^{-5} mbar.

The coating unit system was used to deposit the ohmic contact metal which is the back electrode of Schottky diode. The aluminum metal was choose as an ohmic contact with the c-Si layer, where the aluminum will be deposit easier and have a small series resistance. Then an aluminum layer was deposited in a thickness about 0.2 µm and 473 K

2.9 Thickness Measurement

Vacuum deposited films used for electrical, optical or other purposes must normally be deposited to specified thickness.

In this part two experimental methods of thickness measurements were used: -

2.9.1 Weighting Methods.

A given film thickness may be obtained by the simple formula [33]:

$$th = \frac{m}{2\rho_m \pi R^2} \qquad \ldots (2\text{-}1)$$

Where th is the film thickness in µm, m is the mass of the materials to be evaporated in g, R is the source (boat) to substrate distance and ρ_m is the density of material to be evaporated. This method gives estimate deposited film thickness that is safe to work with it. Figure (2-5) illustrates the idea of this method.

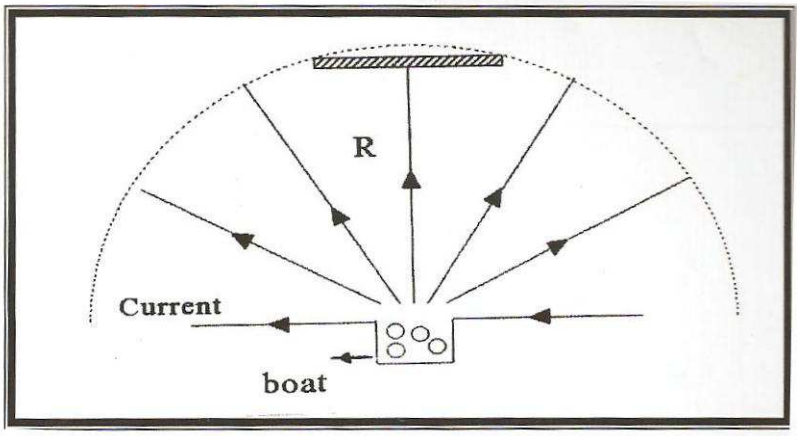


Fig. (2-5) The idea of weighting method

This technique often gives rough estimate results, because there are practical difficulties in evaporating a complete charge from a source and in preventing evaporate losses by spitting of molten material during degassing. So there are about 20% of evaporate material should be added to the calculated weight to substitute the loss material.

2.9.2 Optical Interference Fringes.

Wiener (1887) was the first to measure the thickness of thin films, using optical interference fringes. His method is an application of Fizeau fringes of equal spacing. Donaldson and Khamasavi used the multiple beam interferometric method for precise measurement of film thickness. Tolansky (1948) has given detailed attention to the various factors influencing fringe width and has shown that for the production of highly sharpened multiple beam Fizeau fringes [33]:

1. The surface must be coated with high reflecting films.
2. The film must be uniform thickness.
3. The air gap between the flat and specimen surface must be as small as possible (less than 0.01 mm).
4. The angular spread in the incident parallel beam less than 1º to 3º.
5. The incidence beam should be normal.

Fizeau fringes of equal thickness are obtained in an optical apparatus of the type shown in Figure (2-6). The film thickness (*th*) is given by:

$$th = \frac{\lambda}{2}.\frac{\Delta x}{x} \qquad \text{..... (2-2)}$$

Where ΔX is the shift between interference fringes, X is the distance between interference fringes and λ is the (Na) wave length (5893 Å).

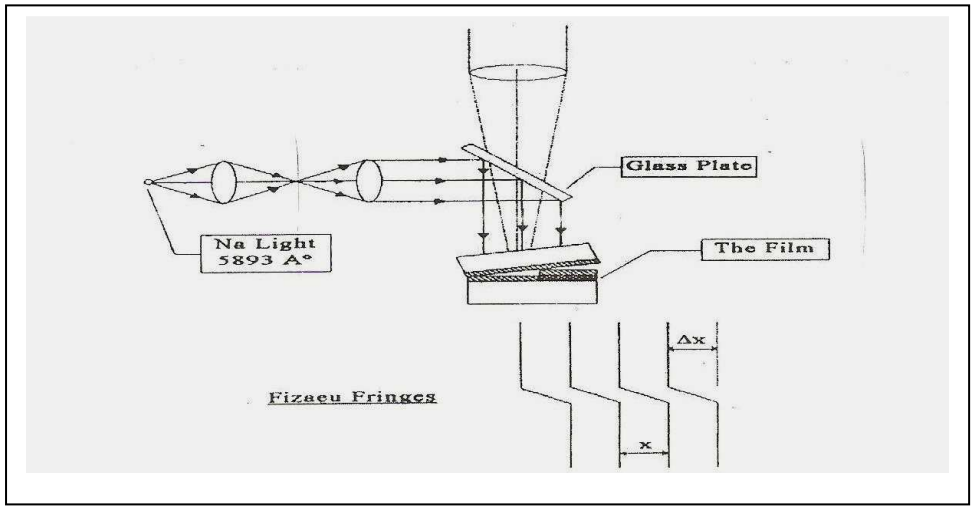


Fig. (2-6) Optical interference fringes method [33].

2.10 Measurement of Schottky Diodes

2.10. 1 Current – Voltage Measurement

This point take measure current as the function of the applied voltage on both ends of the Schottky diode using the consider devices

1-Keithly 616 Digital Electrometer

2-Power supply 1540 D.C 40-300A

3- Philips Multimeter with 10^{-14} resolution

4- Comark Digital Thermometer 500

I-V characteristics of Al/c-Si/In, Al/c-Si/Ag, Al/c-Si/Au Junctions in reverse and forward bias was made by d.c power supply and two digital

electrometers type Keithly. as in Figure (2-7), and then we plot the forward current as a function of bias voltage.

From I-V measurements we can determine the potential barrier height (ϕ_B) the reverse saturation current (J_s) and ideality factor of the diode (n).

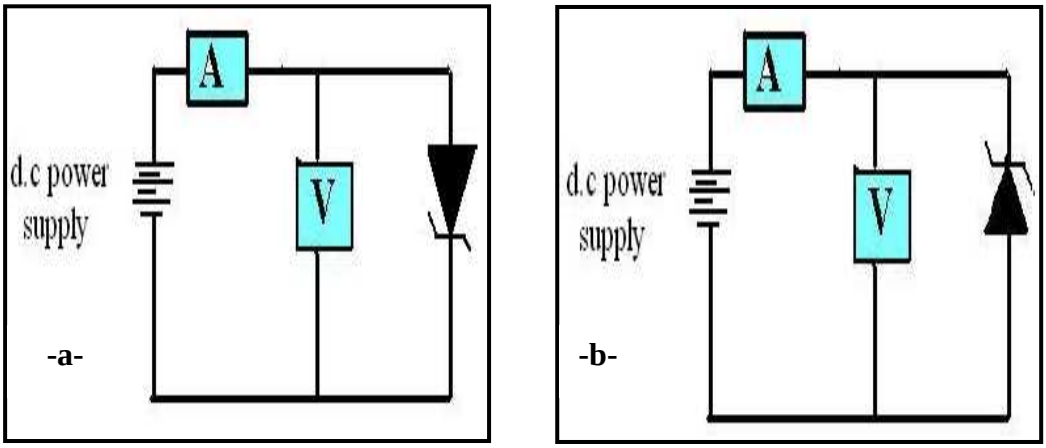


Fig.(2-7) circuit diagram of I-V measurement under a- forward b- reverse bias

Ideality factor can be determined from the slope of ln J – V graph in the linear region, the J_s values were obtained by extrapolating the linear portion of the forward bias ln J - V plot of the intercept point on the current axis at zero bias (V=0) using equation (1-4), (1-6) respectively. Height of barrier can be determined from equation (1-7)

2.10.2 Current – Temperature Measurement

Put the diode in a furnace, and apply a constant voltage on both diode ends and record current values are function for the temperature that recorded by using a double thermal putting in touch with the diode, the measurements have been done with sensitive digital electrometer type Keithly 616 and electrical oven.

The study of the temperature dependence of electrical conductivity offers a lot of information about the correlation between the structure and the electrical properties of the films.

The D.C. conductivity has been studies as a function of 1000/T at R.T. and annealing temperatures (373,473) K, under vacuum, and various thickness (0.1,0.2)μm.

And calculate the E_a from different temperature averages. From drawing Ln J relation ship with 1000/T by application of the equation [34]:

$$J = J_s \exp\left[\frac{-E_a}{k_B T}\right] \quad \text{..... .....} \qquad (2\text{-}3)$$

$$E_a = Slope \times k_B \quad \text{.....} \qquad (2\text{-}4)$$

2.10.3 Capacitance-Voltage Measurement

The capacitance –voltage technique relies on the fact that the width of the reverse-biased space charge region of a semiconductor junction device depends on the voltage.

The capacitance of Schottky diode in depletion region can be obtained from equation (1-8)[14].

A plot of C^{-2} versus V gives a straight line, The linearity in plot of C^{-2} versus V indicates that the charge density within the depletion region of the diode is uniform. The value of V_{bi} can be obtained from the intercept of the line that results from plotting between $1/C^2$ on Y-axis as a function of reverse bias on X-axis and carrier concentration can be calculated from the slope of $1/C^2$ versus V plot by means of equation (1-8).

The barrier height can be determined by using equation (1-9)

The Au ,Ag and In films were prepared in sandwich configuration between c-Si and Al thin films electrodes using masks as shown in Figure (2-8a). The measurements were done using "LCR meter type Agilent 4294A precision impedance analyzer". Figure (2-8b,c) illustrates the setting up the test circuit and the front panel of the LCR meter.

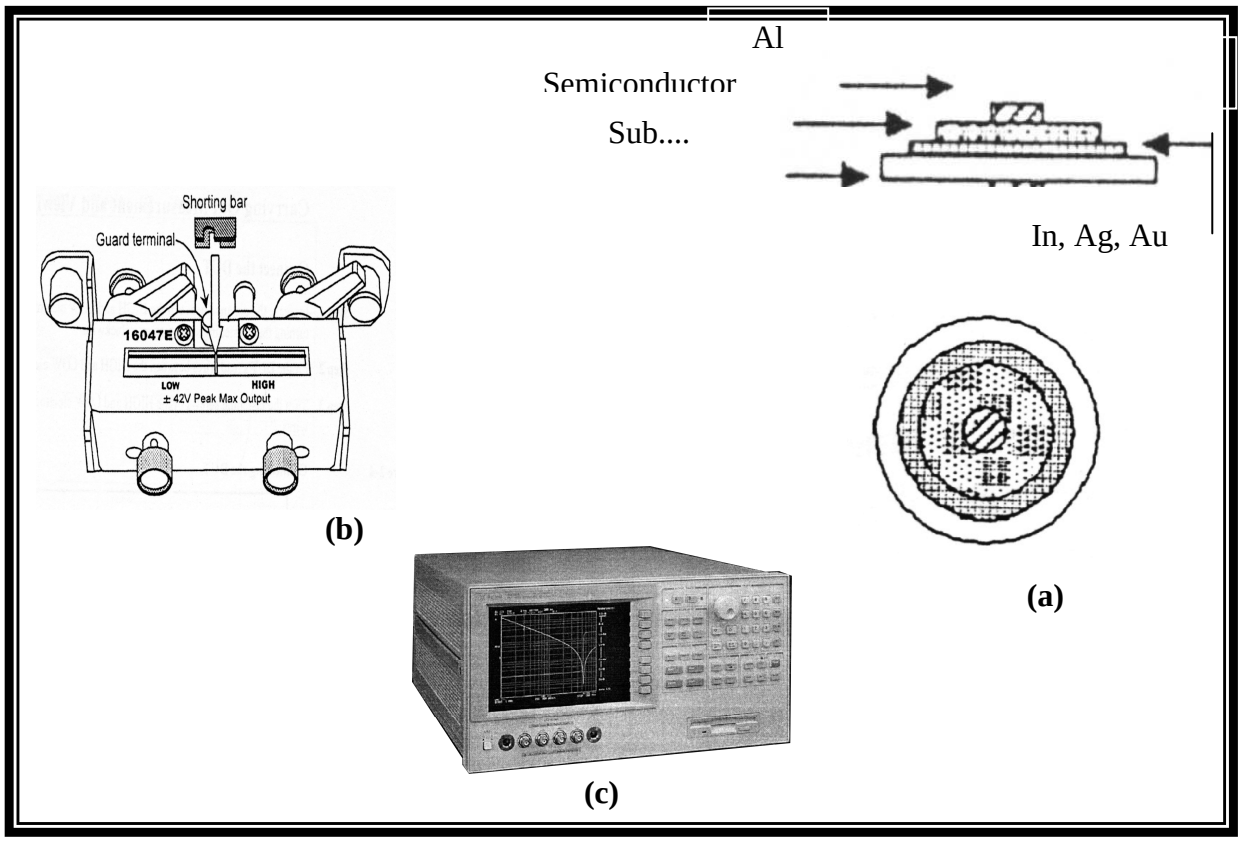


Fig.(2.8) (a) Mask that be used for C-V characteristics, (b) The test circuit, (c) 4294A Precision Impedance Analyzer.

2.11 Current–Voltage Characteristic under Illumination for the Al/c-Si/In

I–V measurements have been done under illumination for the Al/c-Si/In junction which was prepared with different thicknesses and annealing temperatures. When they were exposed to Halogen lamp type Philips of 120 W with different intensities (32.4–105) mW/cm^2, using Keithly Digital

Electrometer 616, Voltmeter and D.C. power supply as shown in Figure (2–9), under reverse bias voltage, which was in the range (0-0.8) volt.

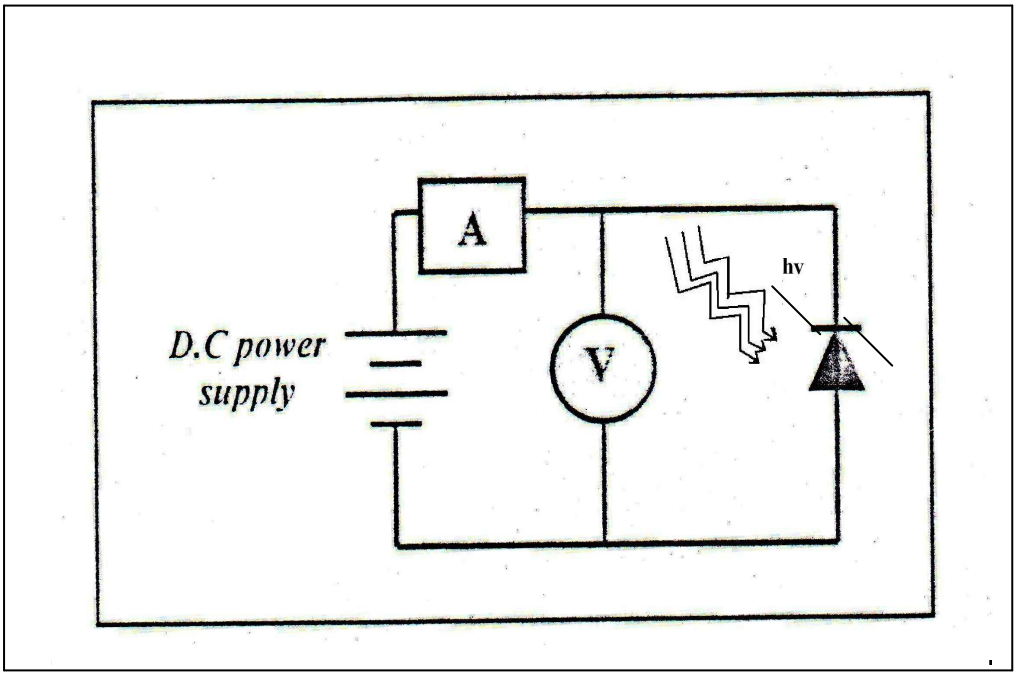


Fig.(2-9) Circuit diagram for I-V measurement of junction under illumination .

Chapter Three

Results and Discussion

3 .1 Introduction

This chapter includes the analysis of results of electrical properties of Al/c-Si/M Schottky diodes as a function of the metal work functions (Al, In, Ag, Au) with different electrode thickness and annealing temperatures. Also we calculate the saturation current density, potential barrier, ideality factor and built in potential from I-V and C-V measurement with different preparation conditions.

The variation of current density as a function of temperature and determination of the transport mechanisms and the activation energies of deposited films are also presented.

3.2 Ohmic Contact of Al/c-Si/Al Junction

Figure (3-1) show that the I-V characteristic of Al/c-Si/Al junction for forward and reverse biasing.

It can be seen from this curve that the linear relation shape behavior between current and voltage for all samples prepared with different thickness and annealing temperatures. The interpretation of this behavior may be that of the work functions of Al and c-Si are nearly similar, that's means the junction not create the depletion layer, $\phi_{B,}$ is zero or negative and electron can flow freely in the two direction. In ohmic contact no potential barrier will be formed between Al electrode and c-Si layer. These results are in agreement with Hussein [35].

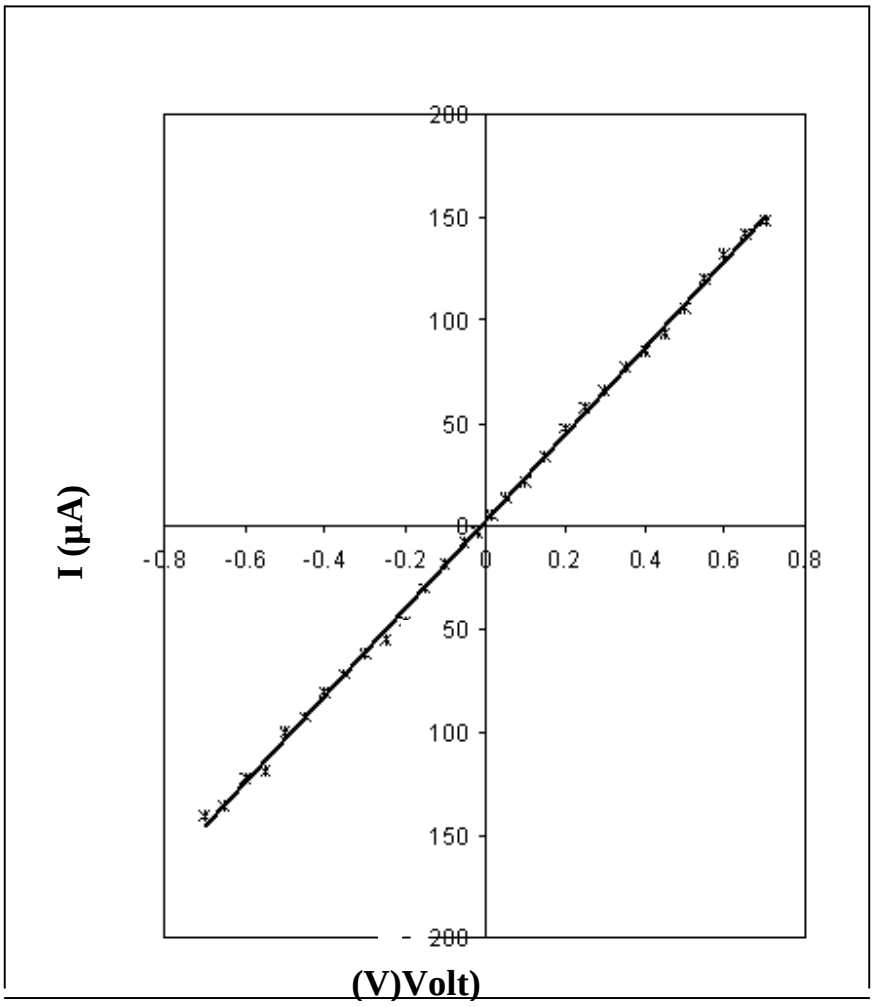


Fig.(3-1) Relation between current and voltage for Al/c-Si/Al ohmic contact at 473K and thickness 0.2µm

3.3 I- V Characteristics of Al/c-Si/M Schottky Diodes

One of the important parameters of diode measurement is a current - voltage characteristic which explains the behavior of the resultant current with the applied forward and reverse bias voltages, in general, is due to the flow of majority charge carriers over the barrier by a thermionic process.
The electrical characterization of a Schottky diode necessitates the determination of the barrier height, ideality factor and saturation current density.

Figures (3-2), (3-3) and (3-4) show (Ln I-V) characteristics for Al/c-Si/In, Al/c-Si/Ag, and Al/c-Si/Au, respectively at forward and reverse bias voltage for different thickness and annealing temperatures.

The current rise slowly with the applied reverse bias and does not show any effect of saturation. This soft or slight non saturation behavior of reverse current may be explained in terms of the image force lowering of Schottky barrier height, presence of the interfacial insulator layer at metal-semiconductor interface and thermionic emission theory does not the dominant mechanism of current transport in our measurements. Similar observation were observed by Raheem [36], Salma [37] and Rahman [38].

The non linearity of the (Ln J-V)characteristics of the Schottky diode at high bias values indicates a continuum of interface states, in which at equilibrium with semiconductor and the non-linearity of the LnJ-V characteristics indicates that the prevalent conduction mechanism is non-ohmic in nature and it may reveal the existence of different kinds of conduction mechanisms. The curves show the good rectifying nature of the

device indicating the presence of barriers on the device. The current slightly increases with increasing of the applied voltage. For comparison Figures (3-2) and (3-3) show that at a fixed voltage, the magnitude of current (I) decrease with increasing electrodes thickness which is attributed to evolving defects and dislocations that have effect on mobility of charge carrier. Also these defects evolutions allow energy levels to be within the energy gap, these defects are within the depletion region and act as active recombination centers, and consequently they decrease current flow across the junction [39].

From the Figures, we can observed that at a fixed voltage, the magnitude of current (I) decrease and then increase with increasing annealing temperature which attributed to increase and then decrease in the depletion width, and to improve in crystal structure by increase and decrease in the crystalline grain size.

We are plotted the ln J–V characteristics with semi logarithmatic scale for the current to estimate the saturation current density (J_S), the ideality factor (n) and the effective barrier height (ϕ_B). The J_S values were obtained by extrapolating the linear portion of the forward bias ln (J)-V plot to the intercept point on the current density axis at zero bias (V=0).

Table (3-1) exhibits the values of saturation current density of Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au at the different thickness and annealing temperatures. From the Table the values of saturation current density are smaller due to the effect of the increasing thickness of the semiconductor layer, which completes the electrons to tunnel through the additional barrier.

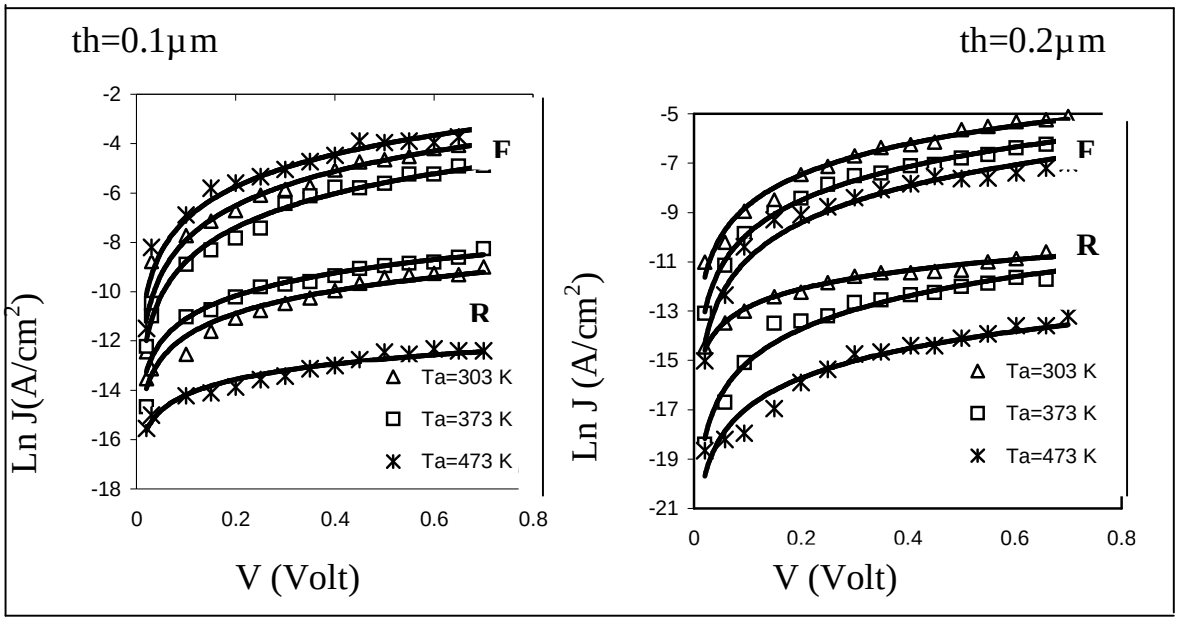


Fig.(3-2) LnJ-V characteristic for Al/c-Si/In at forward and reverse voltage at different thickness and annealing temperatures

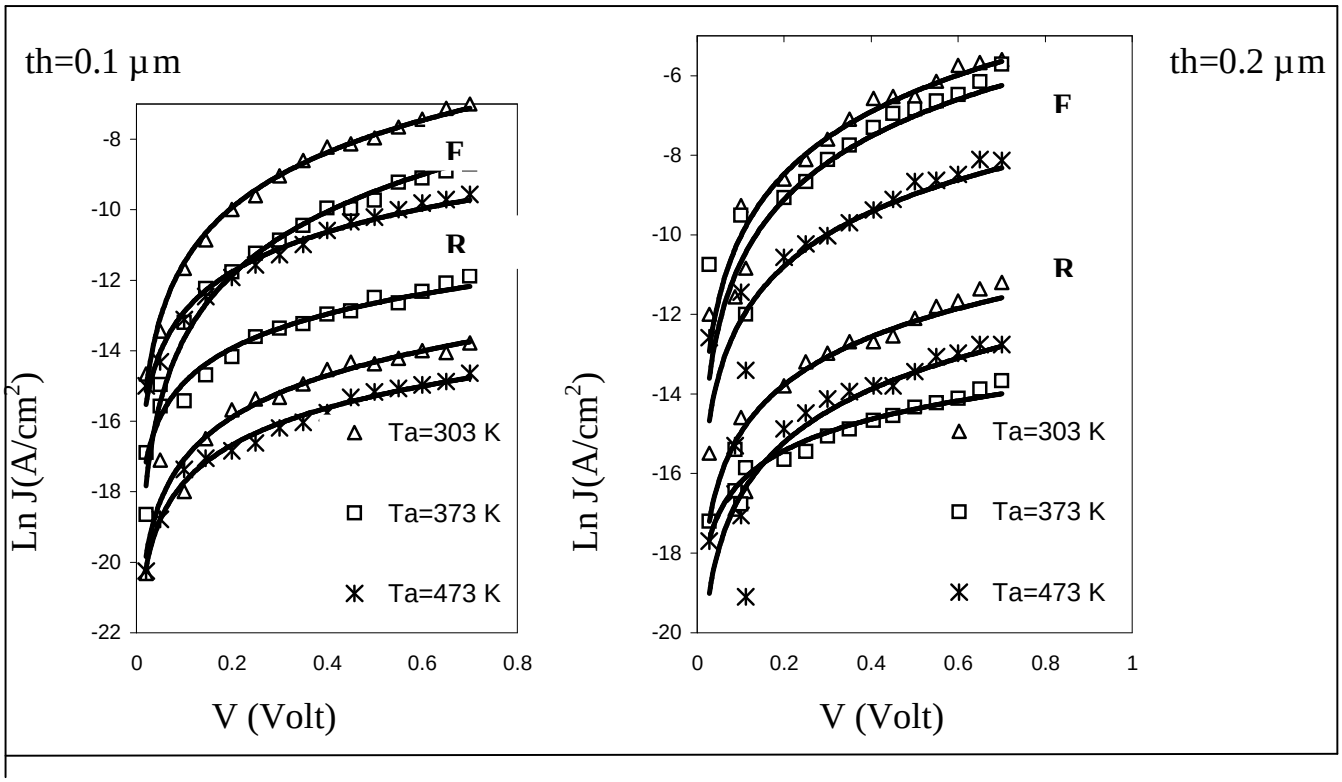


Fig.(3-3) LnJ-V characteristic for Al/c-Si/Ag at forward and reverse bias voltage at different thickness and annealing temperatures.

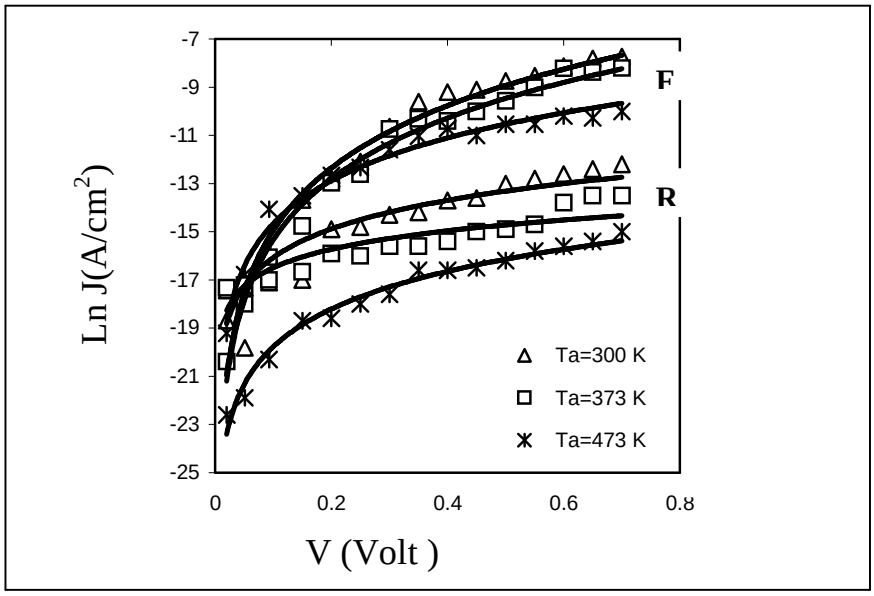


Fig.(3-4) LnJ-V characteristic for Al/c-Si/Au at forward and reverse bias voltage at thickness0.2µm and annealing temperatures.

Also, from the Table (3-1), we found that the values of the ideality factor for Al/c-Si/In and Al/c-Si/Ag samples larger than unity and close to unity for Al/c-Si/Au samples, the ideality factor values for ideal diffusion current is equal to one, whereas, ideality factor values for recombination current is greater than unity. The increasing in (n) values indicates that the junction was non-ideal and most of the carriers (electrons and holes) were recombined at the junction (depletion region). On other hand, there can be many reason to get junction ideality factor greater than unity; Bayhan and Ercelebi [40] attributed the increase of (n) to the series resistance effects which are associated with the neutral region of the semiconductor (between depletion layer and ohmic contact), Rahman [38] attributed to the presence of an interfacial layer and tunneling effect.

Table (3-1) I-V characteristics for Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au at different thickness and annealing temperatures.

	th(μm)	T_a (K)	$J_s \times 10^{-5}$ (A/cm^2)	n	$\phi_B(IV)$ (eV)
Al/c-Si/In	0.1	٣٠٣	٨٢	٤,٧	٠,٥٧
		٣٧٣	٣٠	٤,٣	٠,٧٤
		٤٧٣	٢٣	٤,٢	٠,٩٨
	0.2	٣٠٣	٨,١	٤,٥١	٠,٦٣
		٣٧٣	٤,٩	٤,٢٩	٠,٨
		٤٧٣	٣,٥	٤,٠١	١,٠٥
Al/c-Si/Ag	0.1	٣٠٣	٢,١	٣,٧٠	٠,٦٦
		٣٧٣	٢,٠	٣,٥٥	٠,٨٣
		٤٧٣	٠,٤٤	٣,٢٣	١,١٤
	0.2	٣٠٣	٠,٥٢	٣,٥٥	٠,٧
		٣٧٣	٠,١٣	٣,٥١	٠,٩٢
		٤٧٣	٠,٠٩	٣,٤٩	١,٢
Al/c-Si/Au	0.2	٣٠٣	٠,٠٠٨١	١,٩٨	٠,٨٥
		٣٧٣	٠,٠٠٥٨	١,٨٣	١,٠٦
		٤٧٣	٠,٠٢٤	١,٤٣	١,٣١

From Table (3-1) and the same Figures we can observe that there is an increasing in the barrier heights with the increasing of the annealing temperatures the probable reason for this increasing is that metals disperse intimately during annealing and ensure a chemical reaction at the interface between the metal and the semiconductor where the surface states in the mobility gap and the interfacial layer will reduce between the Silicon and metal . Lalinisky et al [41] found that there is an increasing in the barrier height with increasing the annealing temperature; this because of the interfacial layer will disappear through the annealing process.

From the Figures we found that the rectification ratio increase with increasing annealing temperature this may be reduce of defect of the interface layer.

The rectification ratio 10^3 (three order) for Al/c-Si/In at (473) K while decrease to 10^1 (one order) for Al/c-Si/In at (303) K. From the Figures we found that the rectification properties dependence on the work function of the metal (Schottky contact), for the three diodes which are prepared by thermal evaporation at different annealing temperatures. We found that the rectification ratio of Al/c-Si/Au greater than 10^4 (four order) at (473) K.

The rectification properties of Al/c-Si/Au junction are larger than that of Al/c-Si/Ag and Al/c-Si/In junction (larger barrier height, smaller reverse saturation current density and smaller ideality factor) because of the difference between their work function as well as the oxygen at the interface appears to have small effect on the Al/c-Si/Au barrier height [3].

Figures (3-5), (3-6) and (3-7) shows the ideality factor exhibits an decrease with increasing temperatures and increasing thickness, and the same Figures shows saturation current density decrease with increasing

temperature because of chemical reaction at the M/c-Si interface, and the decrease of J_s with increasing annealing temperature at thickness (0.1, 0.2) µm may be due to increase the junction resistance (increase of the depletion width), these results were similar to Singh et al [42] where they found a decreasing in ideality factors and increasing in ϕ_m with increasing the temperature for Au/Si junction

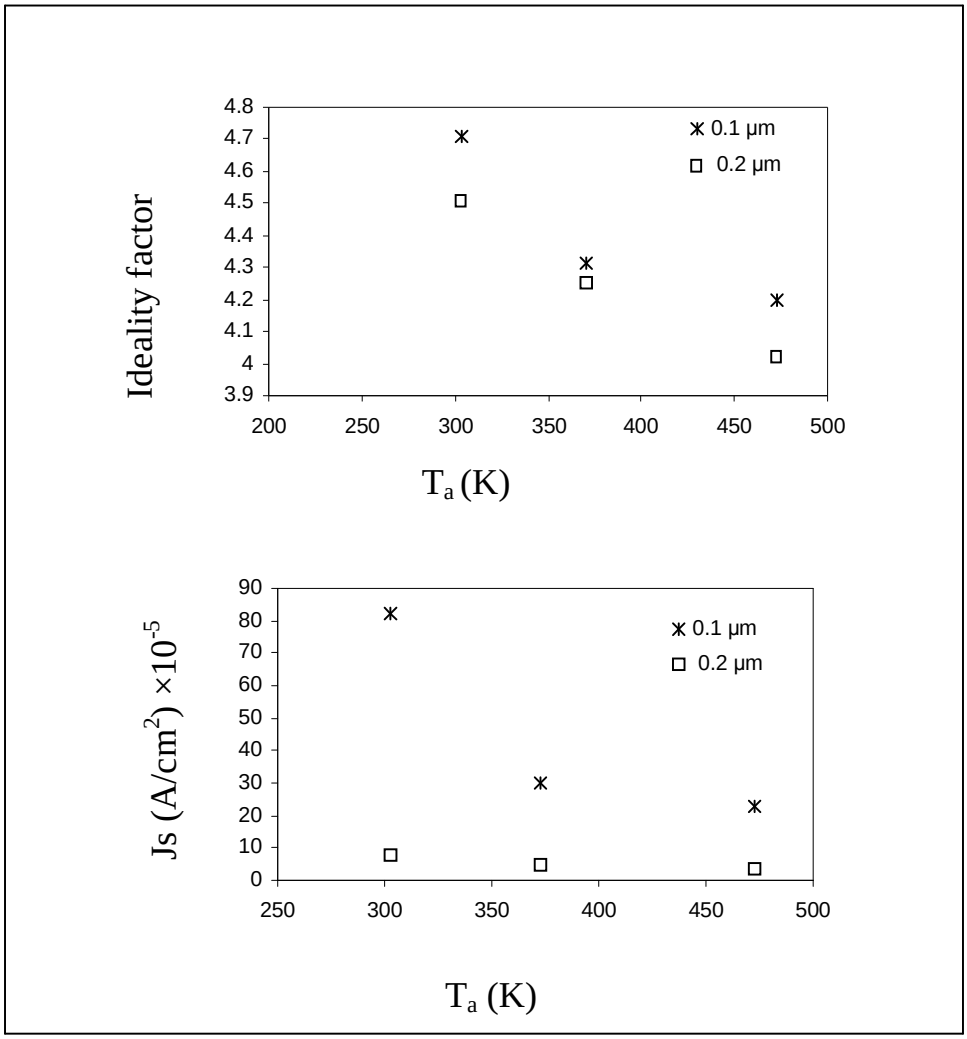


Fig.(3-5) Effect annealing temperatures on ideality factors and saturation current density for Al/c-Si/In

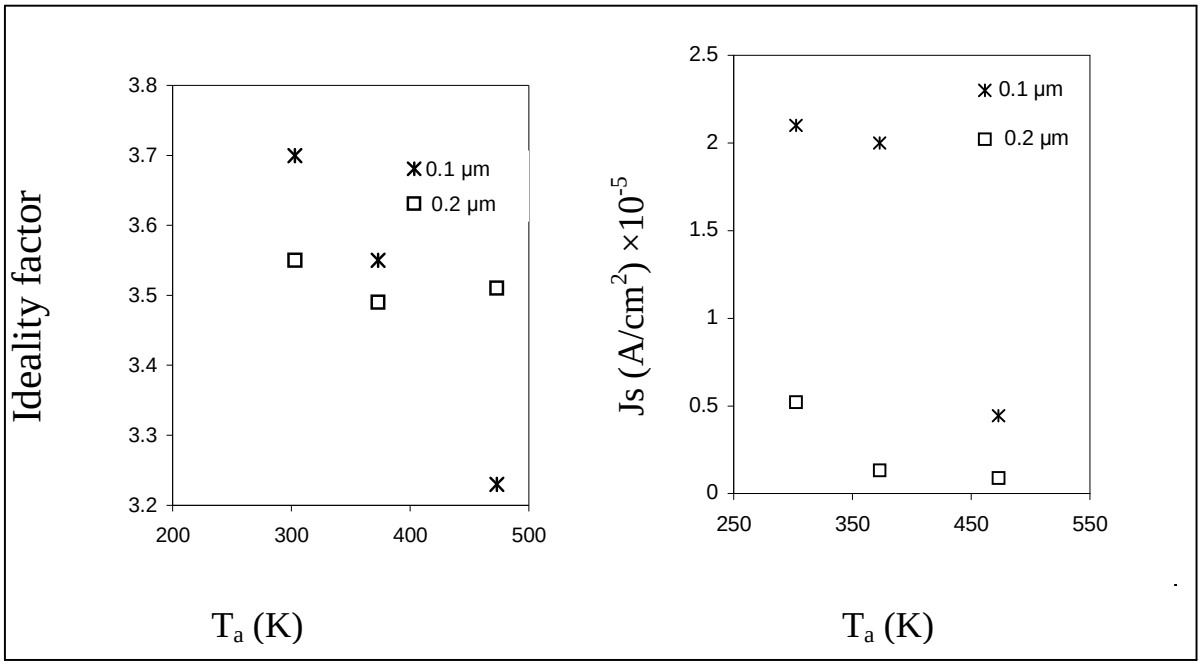


Fig. (3-6) Effect annealing temperatures on ideality factors and saturation current density for Al/c-Si/Ag

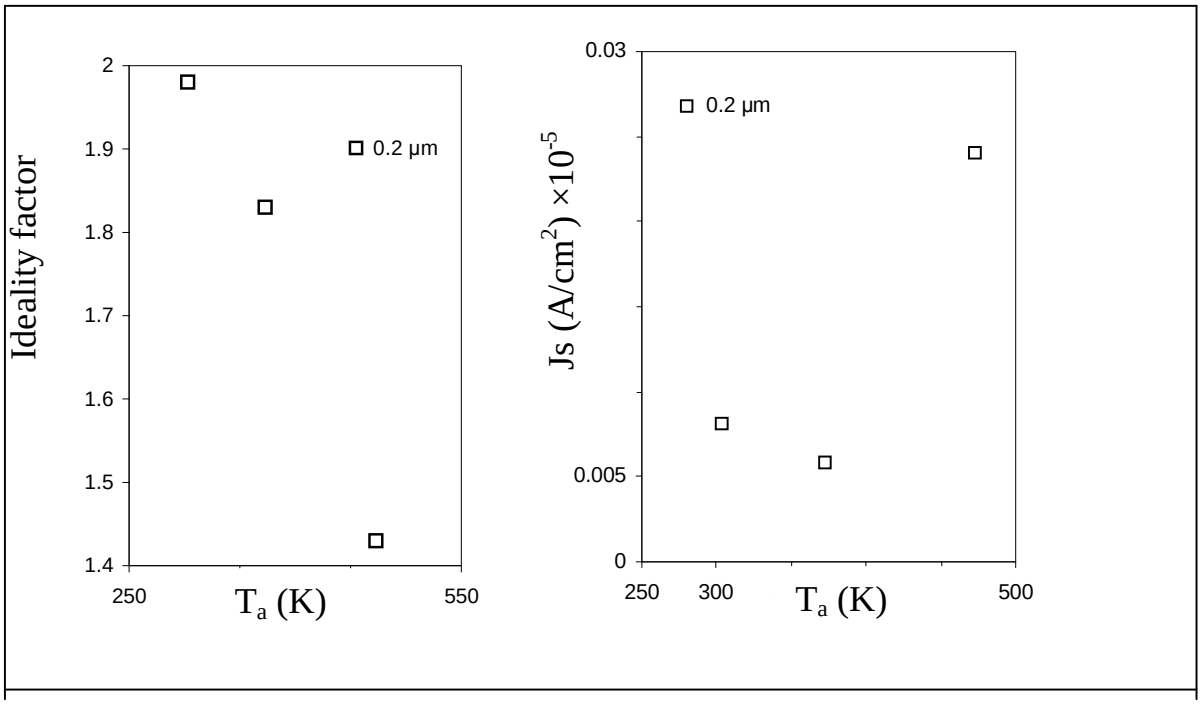


Fig.(3-7) Effect annealing temperatures on ideality factors and saturation current density for Al/c-Si/Au

Figure (3-8) show that the barrier height dependence on the Schottky electrodes, the dependence of ϕ_B on the metal work function with different thermal activation process, electrons at low temperatures are able to surmount the lower barriers and therefore, current transport will be dominated by current flowing thought the patches of lower Schottky barrier height and larger ideality factor.

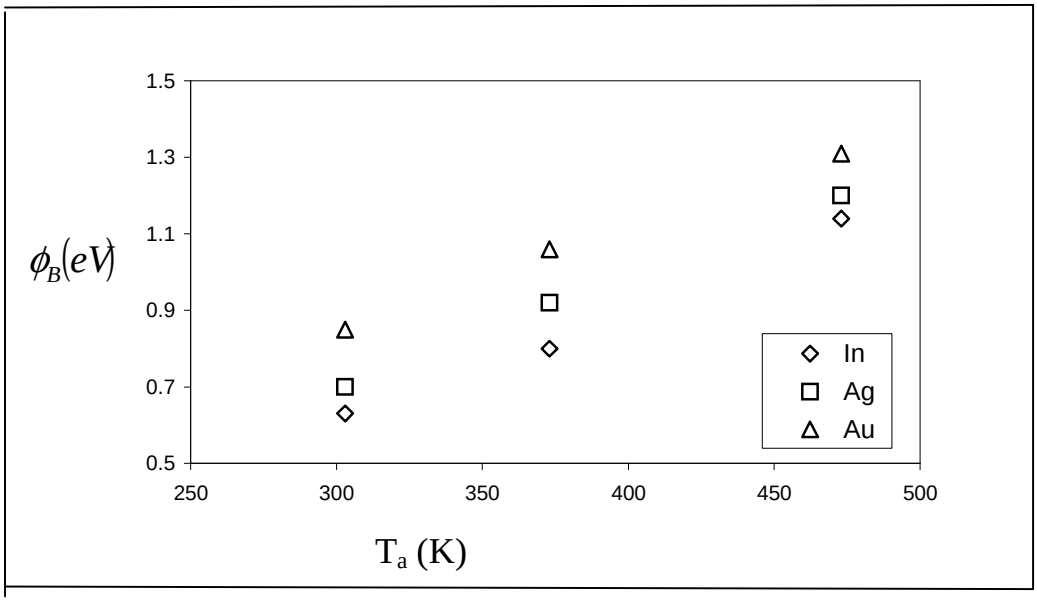


Fig.(3-8)Effect of the work functions and annealing temperature on barrier height .

We can see that the potential barrier (ϕ_B) values increasing with increase the metal work function (ϕ_m) and annealing temperature these results may be attributed from reduced the surface state and dislocation at interface layer, as shown in Figures (3-9)

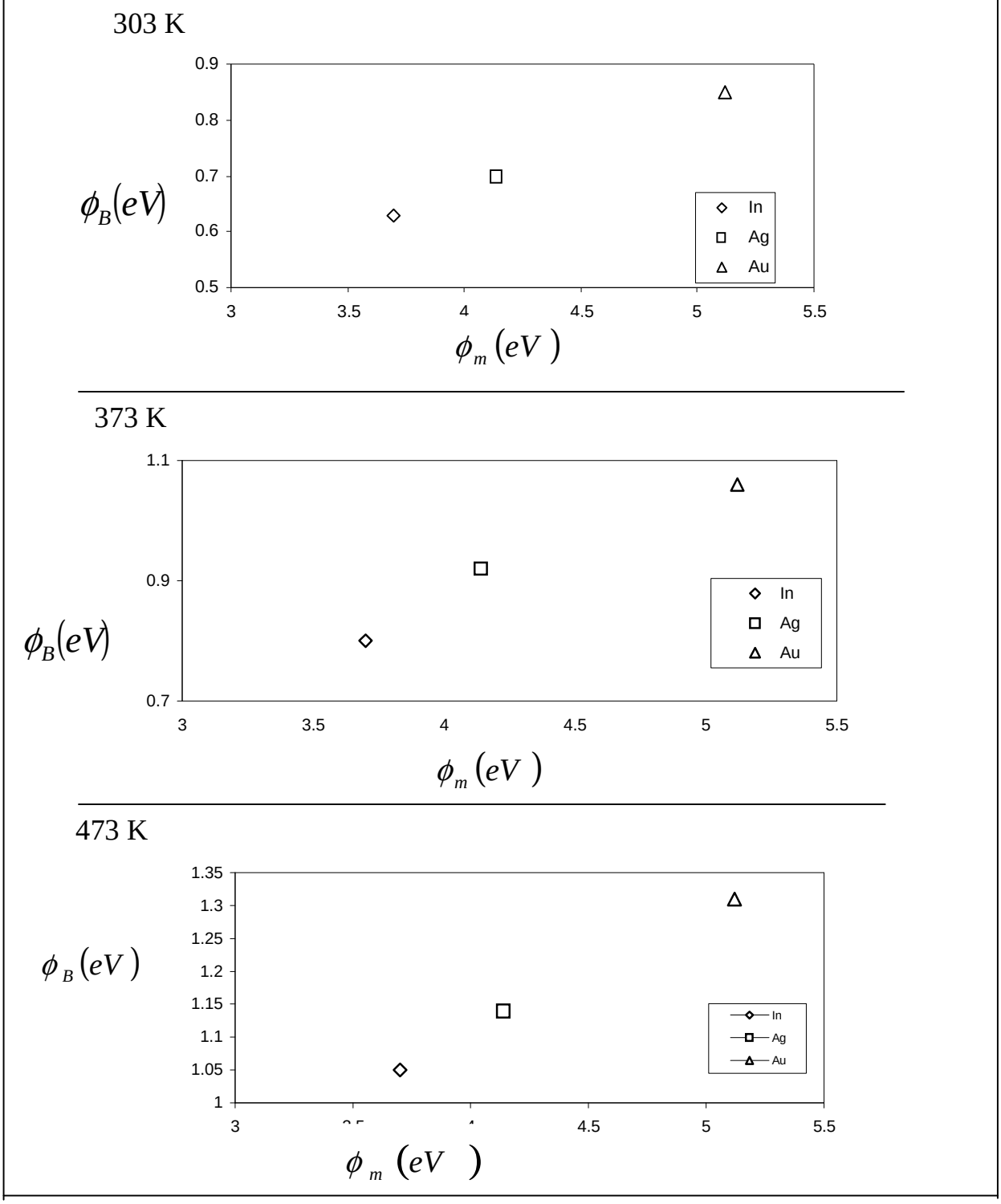


Fig.(3-9) Effect metal work function on barrier height for Al/c-Si/In, Al/c-Si/Ag, Al/c-Si/Au for thickness 0.2 µm

3.4 Capacitance-Voltage characteristics of Al/c-Si/M Schottky Diodes

Capacitance versus voltage, referred to as C-V measurement can be used to study the most basic properties of semiconductor junction. In addition to obtaining simple capacitance values at a given bias. The data can be manipulated to yield a number of other parameters such as the built-in potential (V_{bi}), the doping profile and the barrier height. C-V measurements also form the basis of more advanced analysis techniques such as deep level transient spectroscopy [43].

The variation of capacitance as a function of reverse bias voltage in the range of (0-0.7) Volt at frequency equal to 1 MHz has been studied, for Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au for different thickness and annealing temperatures as shown in Figures (3-10), (3-11) and (3-12) in these in Figures we observe that the capacitance of structure is decrease with increasing semiconductor thickness. This result confirm by equation $C=A\varepsilon_s/th$. Where (A) is the active area of the junction and(ε_s) is the dielectric constant and (th) thickness of semiconductor layer.

It is clear that the capacitance decreases with increasing of the reverse bias voltage and annealing temperatures, the decreasing was non-linear as shown in Figures (3-10), (3-11) and (3-12). Such behavior is attributed to the increasing in the depletion region width, which leads to increase of the value of built– in voltage. This effect has been studied by Nahda [44] and our results are in agreement with their results.

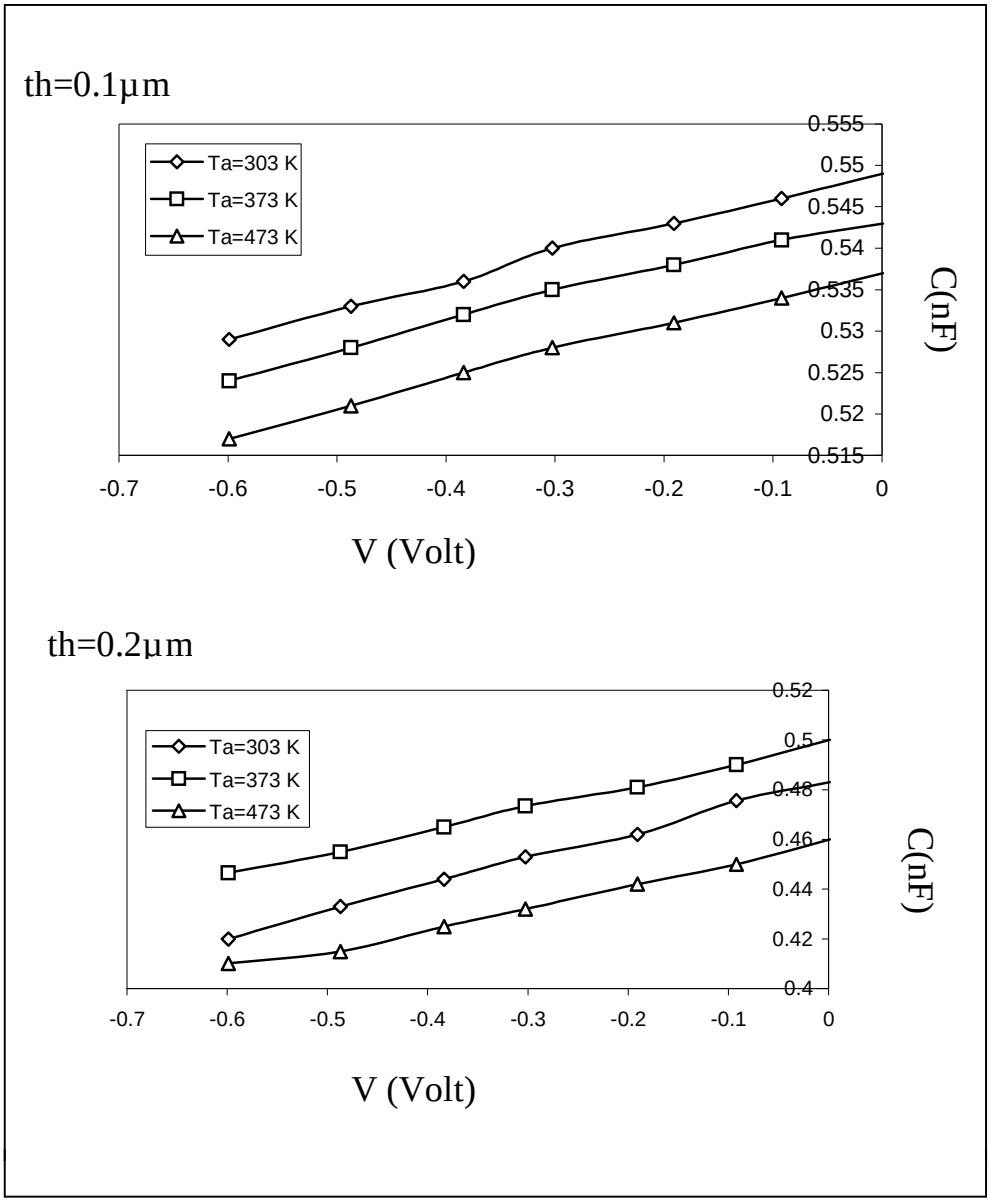


Fig.(3.10) The variation of capacitance as a function of reverse bias voltage for Al/c-Si/In at different thickness and annealing temperatures.

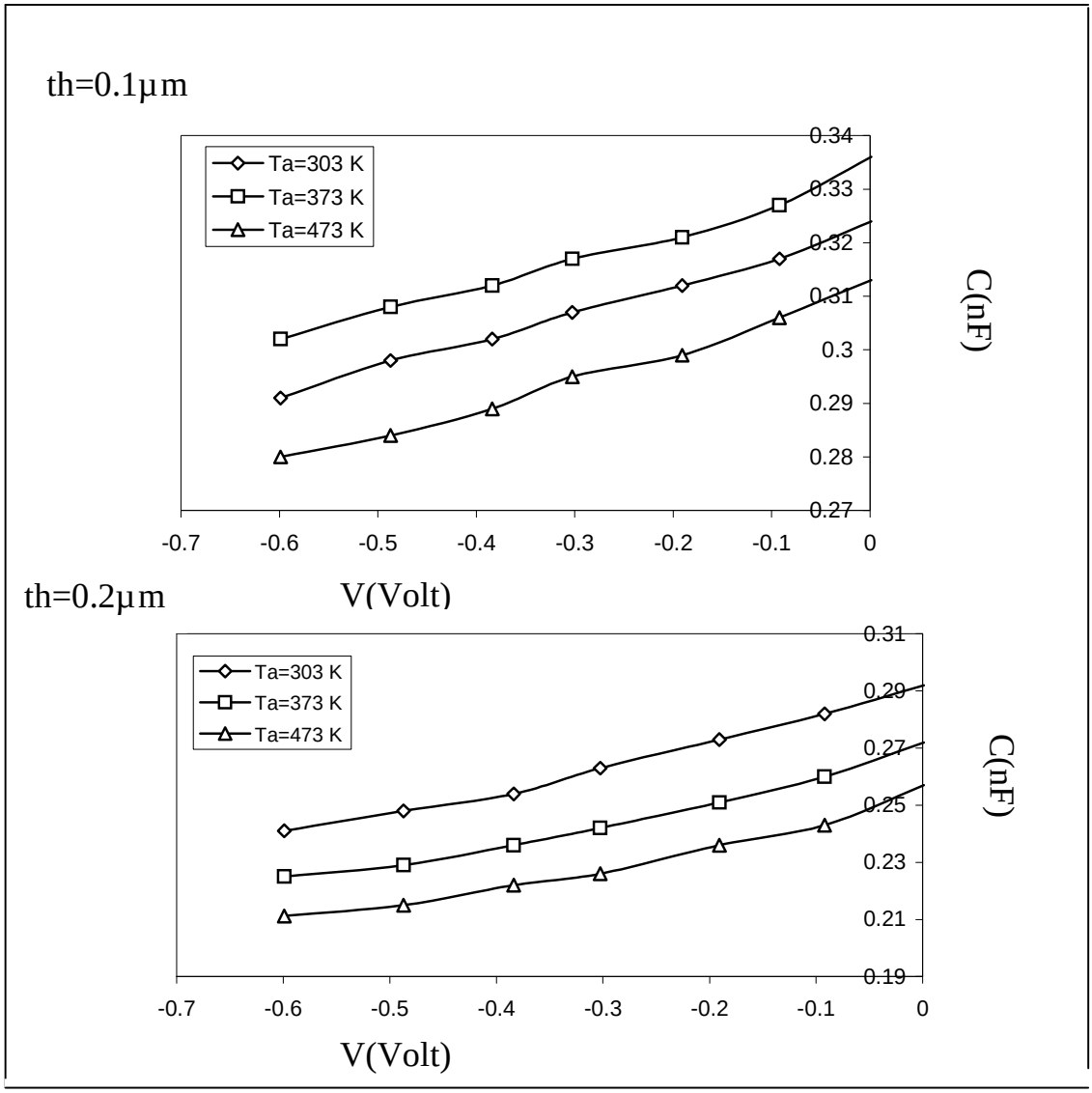


Fig.(3.11) The variation of capacitance as a function of reverse bias voltage for Al/c-Si/Ag at different thickness and annealing temperatures.

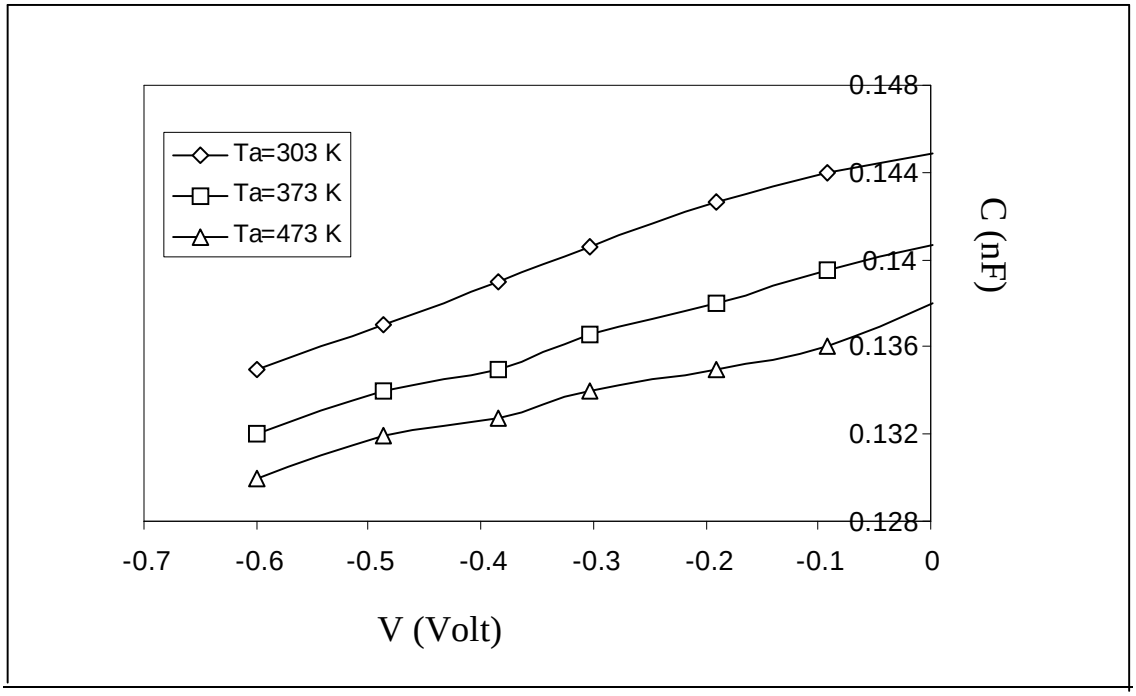


Fig.(3.12) The variation of capacitance as a function of reverse bias voltage for Al/c-Si/Au at 0.2μm and annealing temperatures.

The inverse capacitance square is plotted against applied reverse bias voltage for Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au at different thickness and annealing temperatures as shown in Figures (3-13), (3-14) and (3-15)

The interception of the straight line with the voltage axis at ($1/C^2 = 0$) represents the built in voltage. We observed from Table (3-2) that the built–in voltage increase as a result of the decrease in the capacitance value and the increase of the depletion width.

The slope yields the impurity concentration in the substrates, using equation (1-8). The slope of the curve is inversely proportion to the doping concentration and hence the barrier height (if the shallow level depth is known), using equation (1-9).

The result of built-in voltage, carrier concentration and the barrier height are tabulated in Table (3-2).

We observed from Table (3-2) that the built-in voltage increases with increasing of T_a as a result of the decrease in the capacitance value. Also we can observe that the effect of increasing thickness caused an increase in built-in voltage as given in Table. From the same Figures, we can observe that the effect of increasing thickness caused an increase in built-in voltage as given in Table. From the same Figures, we can notice that the decreasing in the carrier concentration which lead to decrease the capacitance.

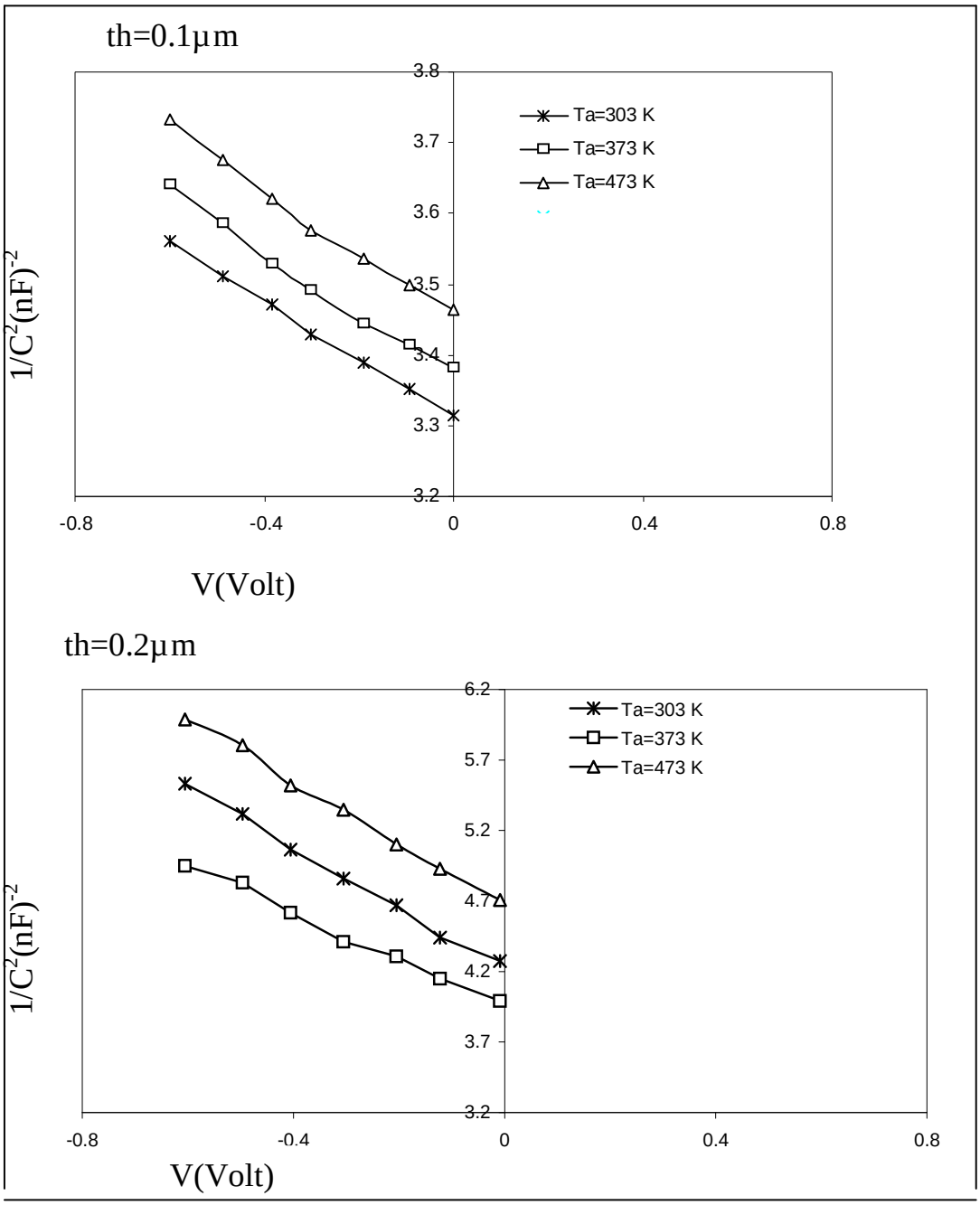


Fig.(3-13) The variation of $1/C^2$ as a function of reverse bias voltage for Al/c-Si/In at different thickness and annealing temperatures.

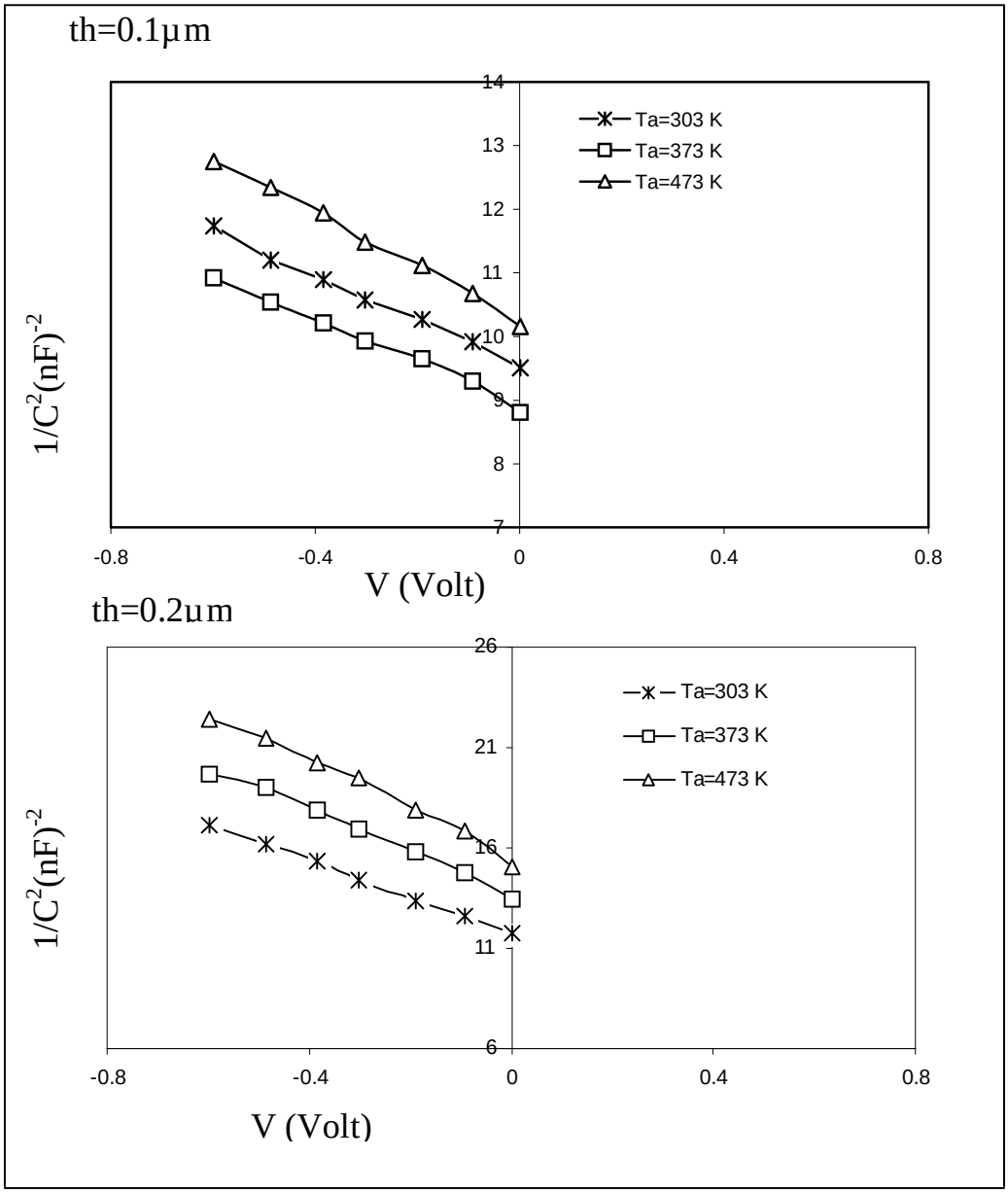


Fig.(3-14) The variation of $1/C^2$ as a function of reverse bias voltage for Al/c-Si/Ag at different thickness and annealing temperatures

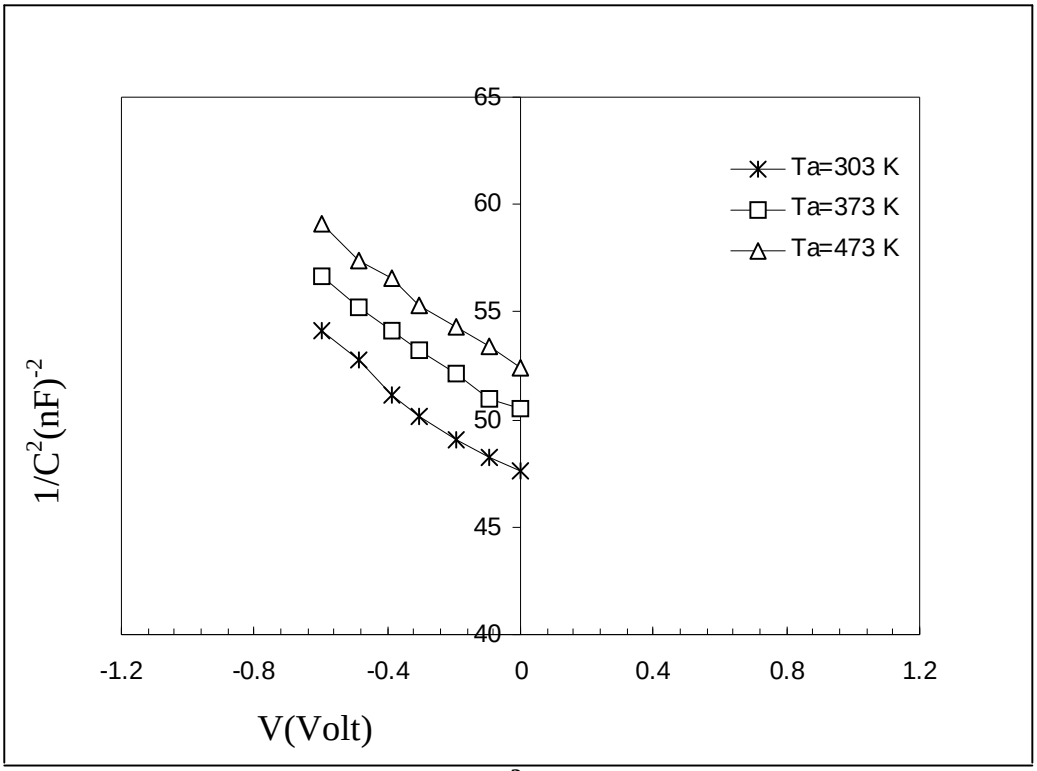


Fig.(3-15) The variation of $1/C^2$ as a function of reverse bias voltage for Alc-/Si/Au at 0.2µm and annealing temperatures.

We can observe from this Figures and Table (3-2) an increasing ϕ_B(CV) are slightly higher than these of I-V and this can be attributed to barrier height lowering due to image force and contribution of tunneling effect.

Table (3-2) The variation of the N_a, V_{bi} and $\phi_B(CV)$ for Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au with different thickness and annealing temperatures.

	th (μm)	T_a (K)	$N_a \times 10^{15}$ (cm^{-3})	V_{bi}(Volt)	$\phi_B(CV)$(eV)
Al/c-Si/In	0.1	٣٠٣	5.79	0.26	0.48
		٣٧٣	5.43	0.4	0.68
		٤٧٣	5.34	0.56	0.89
	0.2	٣٠٣	1.1	0.48	0.65
		٣٧٣	1.43	0.47	0.79
		٤٧٣	1.08	0.65	1.09
Alc-/Si/Ag	0.1	٣٠٣	0.66	0.58	0.84
		٣٧٣	0.70	0.72	1.06
		٤٧٣	0.5	0.8	1.27
	0.2	٣٠٣	0.26	0.59	1.08
		٣٧٣	0.21	0.67	1.05
		٤٧٣	0.19	0.78	1.29
Al/c-Si/Au	0.2	٣٠٣	0.176	0.72	1.006
		٣٧٣	0.187	0.96	1.312
		٤٧٣	0.178	1.1	1.730

3.5 I-V Characteristic of Al/c-Si/In Schottky Junction under Illumination

The photocurrent is the current generated by the absorption of photons. It is considered as in important parameter, which acts on the spectral responsivity.

A photovoltaic effect occurs in a material in which there is a space charge layer. When a photo exited electron-hole pair enters the layer, the electron and hole are separated by the space charge field to give a photo current, the magnitude of the electric field in the space charge region decrease and so the resistivity increases [45].

The relation between the photocurrent (I_{ph}) and reverse bias voltage (V_R) of the Al/c-Si/In structure at different thickness and annealing temperatures are presented in Figure (3-16) and (3-17).). The measurements were carried out under different incident power density equal to (0, 32.4, 55.5, 69,105) mw/cm^2 respectively

From this Figures we observe that the photocurrent increases with increasing of the bias voltage, i.e. I_{ph} increases with increasing of the depletion region width (w) as shown in the relation below

$$I_{ph} = qaG_{ph}\left(L_p + L_n + W\right) \text{..... (3-1)}$$

Where G_{ph} is the generation rate of photo carriers, L_p and L_n are the diffusion length of holes and electrons respectively.

The width of the depletion region increases with increasing of the applied reverse bias voltage. Increasing the reverse bias voltages leads to the increasing in the internal electrical field which leads to an increasing in the probability of the separated electron –hole pairs.

The photocurrent increases with increasing the incident power intensity, due to the increasing in the number of the generated photo carriers in the depletion region with the diffusion depth for carriers which depends on the life time of the minority carriers on the depletion region. From the same Figures we can see that the photocurrent decreases with increasing of films thickness because the created electron-hole pairs may recombine before getting separated by the junction and this is attributed to the increase of the structural defects which leads to decrease of the mobility which in turn decreases the current transfer and leads to short diffusion length. We can notice for all samples that the photocurrent increases with increasing of annealing temperature, which is due to the increasing in the grain size and reducing the grain boundaries which lead to the increase of the mobility and increase the photocurrent as well as increase the depletion width which leads to increase of the absorption through it and the creation of electron-hole pairs [39].

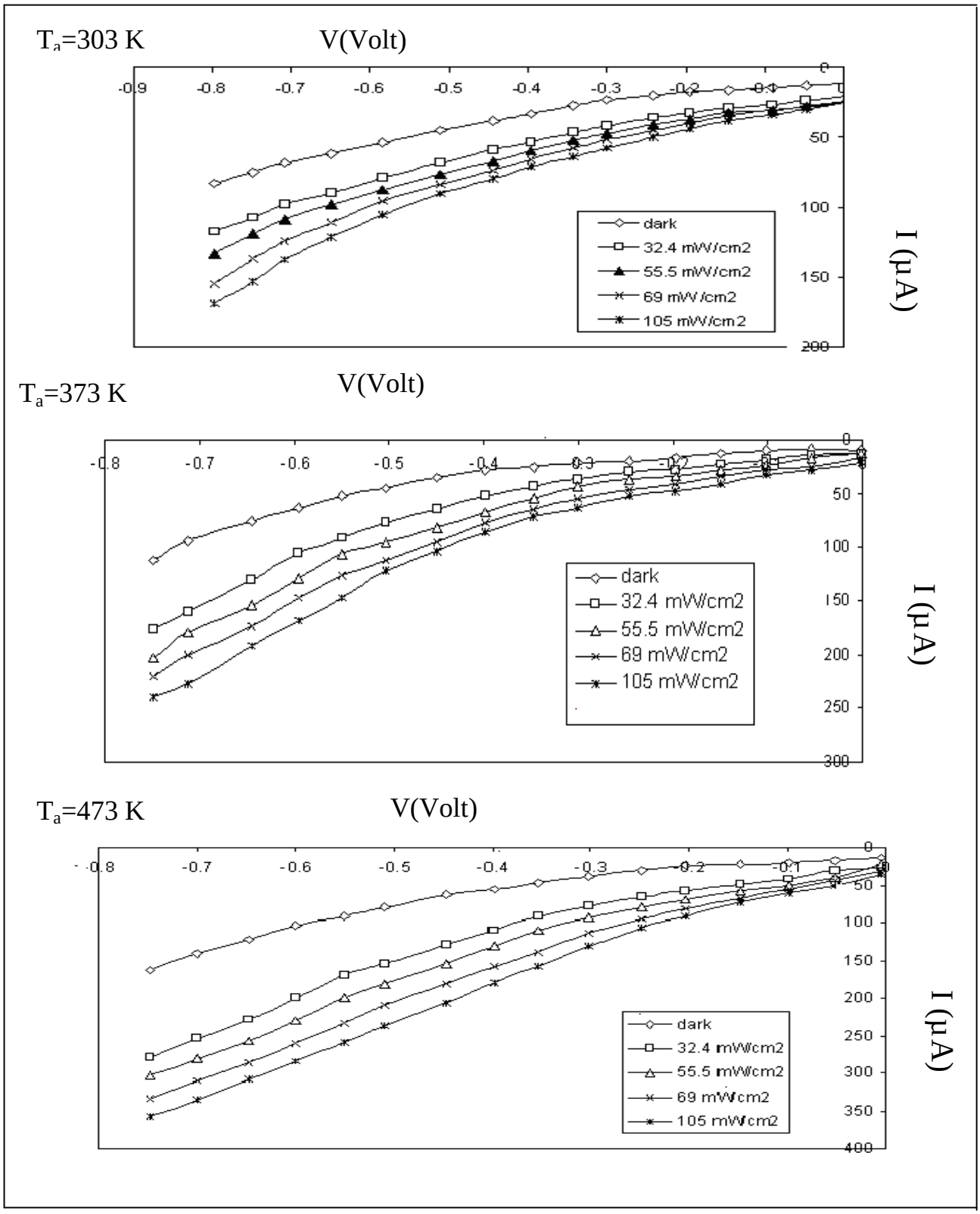


Fig.(3-16) The I-V characteristics under incident power intensity for Al/c-Si/In at reverse bias at thickness 0.1μm for different annealing emperatures.

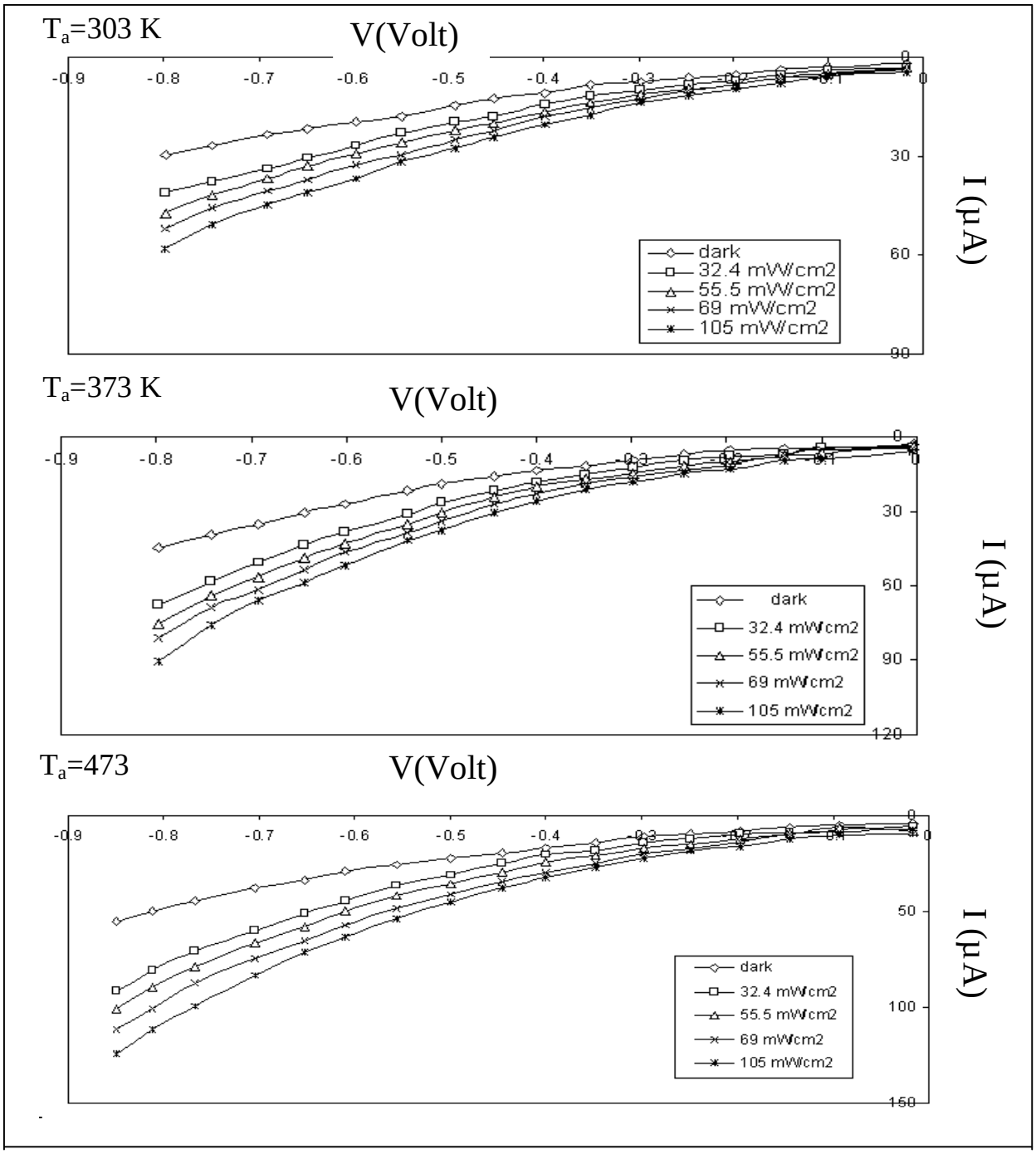


Fig. (3-17) The I-V characteristics under incident power intensity for Al/c-Si/In at reverse bias at thickness 0.2μm for different annealing temperatures.

3.6 D.C. Electrical Conductivity

The variation of electrical current density as a function of temperature at different thickness and annealing temperatures is shown in Figures (3-18) (3-19) and (3-20) It's clear from this Figures that the current density for all deposited films decrease with increase thickness. Also it observed that the current density of the films decrease with increasing of T_a from 303K to 473K, this result is in agreement with Islam and Mitra. [46]. This variation is thought to be due to the changes in crystalline (reduction of the number of grain boundaries due to the increase of grain size).

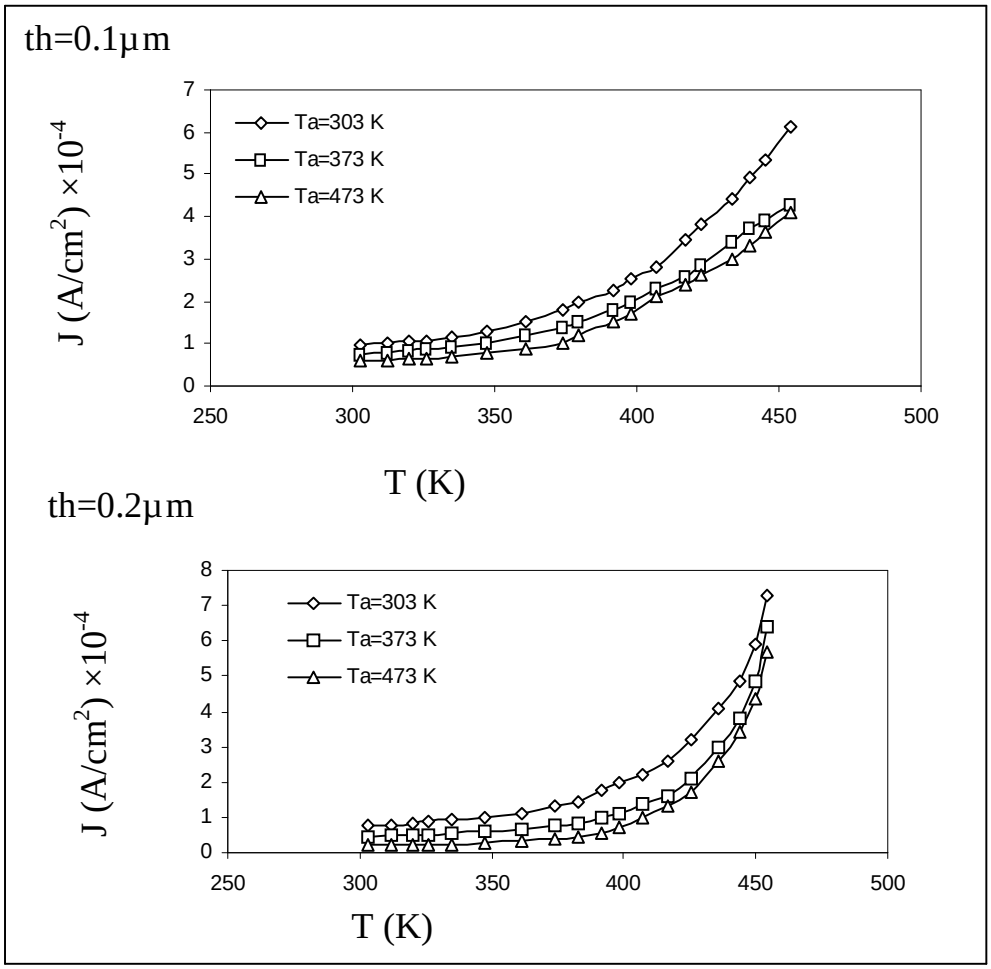


Fig.(3-18) Variation of $J_{D.C}$ versus temperatures for Al/c-Si/In prepared at different thickness and annealing temperatures.

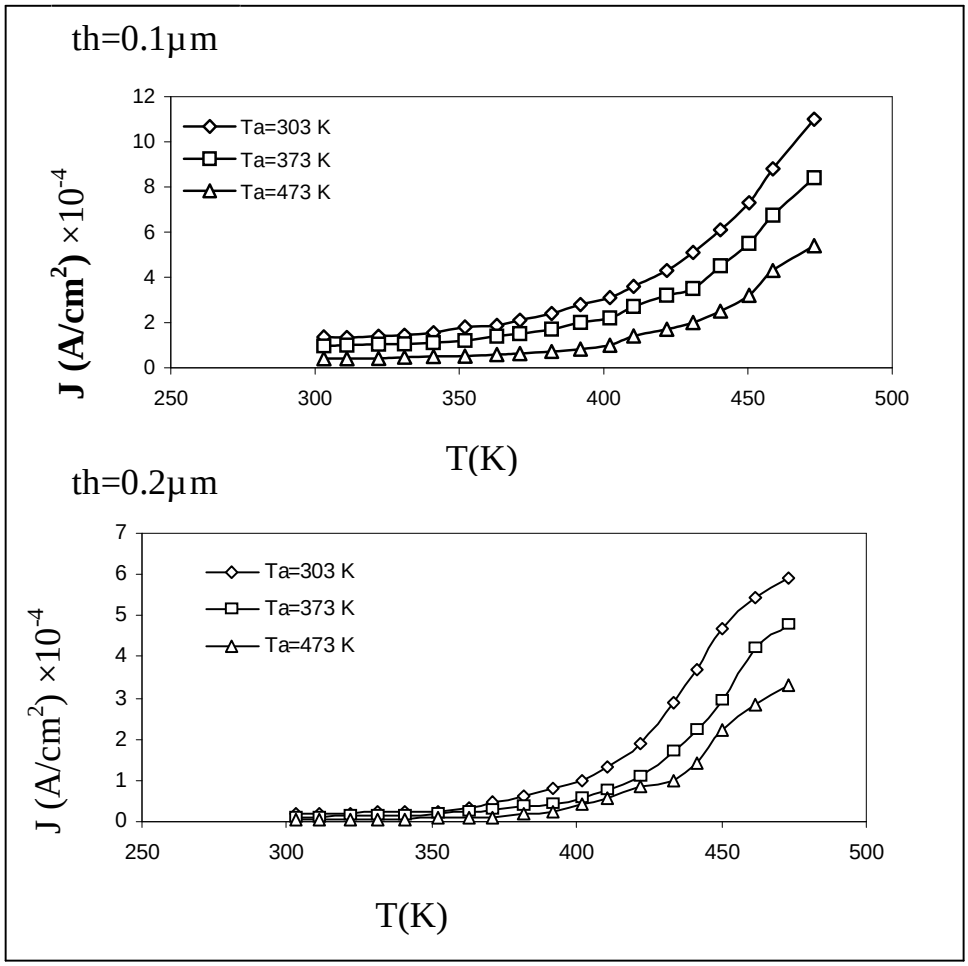


Fig.(3-19) Variation of $J_{D.C}$ versus temperatures for Al/c-Si/Ag prepared at different thickness and annealing temperatures.

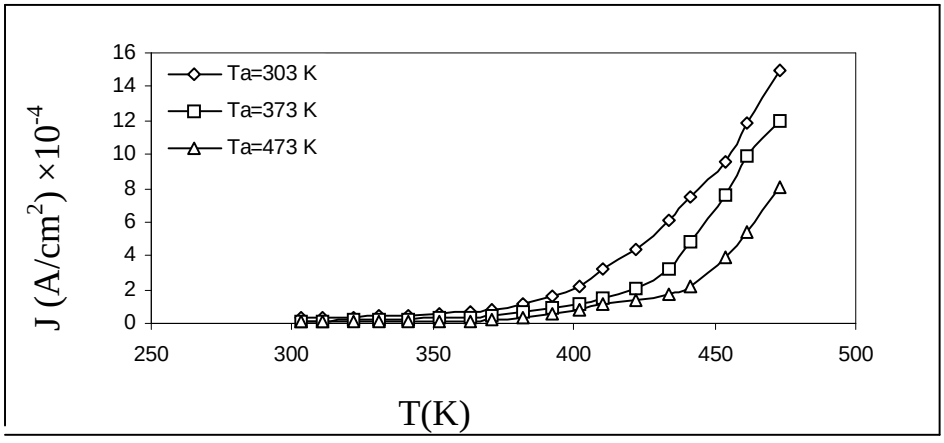


Fig.(3-20) Variation of $J_{D.C}$ versus temperatures Al/c-Si/Au prepared at thickness 0.2µm and annealing temperatures.

It was plot Ln J versus 1000/T to study the dependence of D.C. conductivity for the as-deposited and annealing samples in the range 303 to 473 at different thickness and annealing temperatures, is shown in Figures (3- 21), (3-22) and (3-23). It is clear from these Figures that there are two transport mechanisms, giving rise two activation energies E_{a1} and E_{a2}. At the lower range of temperatures, the conduction mechanism is due to carriers excitation into localized state at the edge of the band and at the higher temperatures, the conduction mechanism is due to carriers excitation into the extended states beyond the mobility edge. Similar observation was reported by Valdez [47].

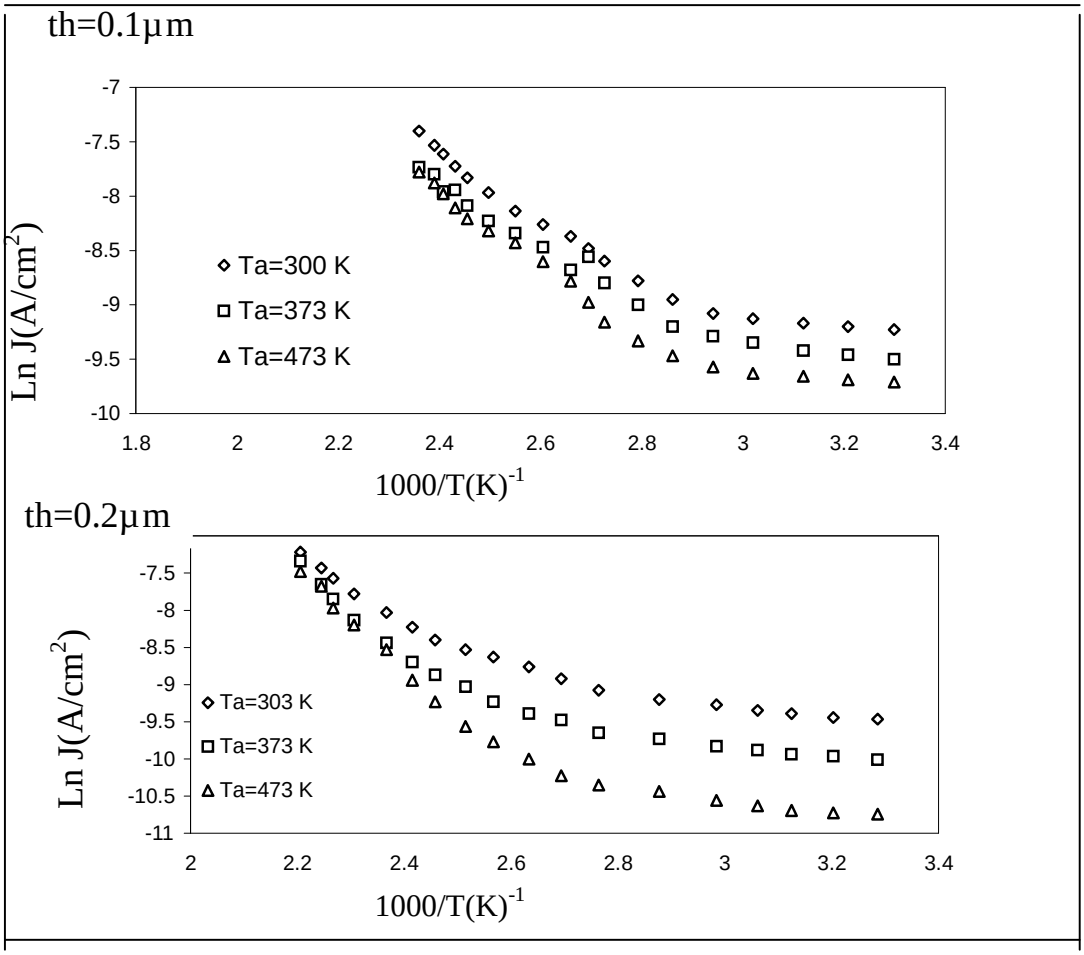


Fig.(3-21)Ln J versus 1000/T for for Al/Si/In at different thickness and annealing temperuters

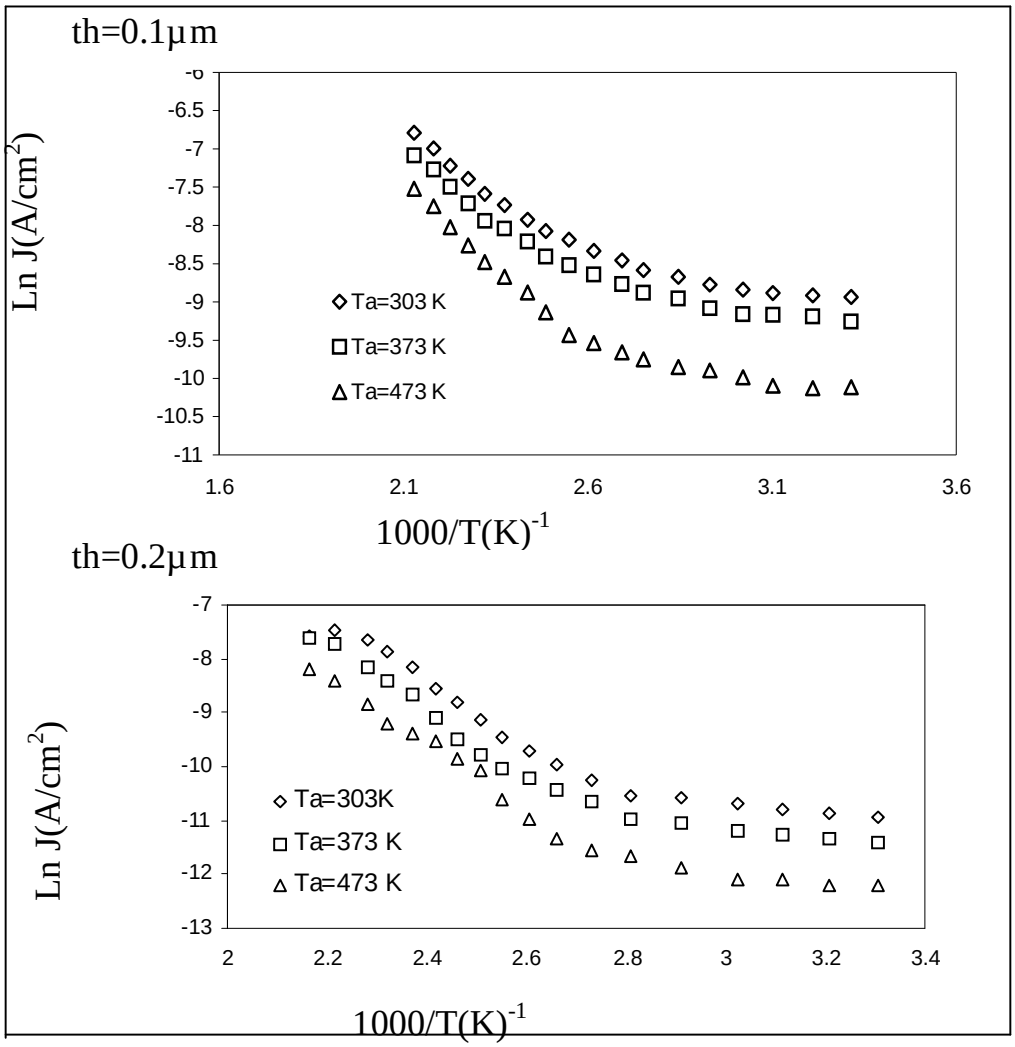


Fig.(3-22) Ln J versus 1000/T for for Al/c-Si/Ag at different thickness and annealing temperuters.

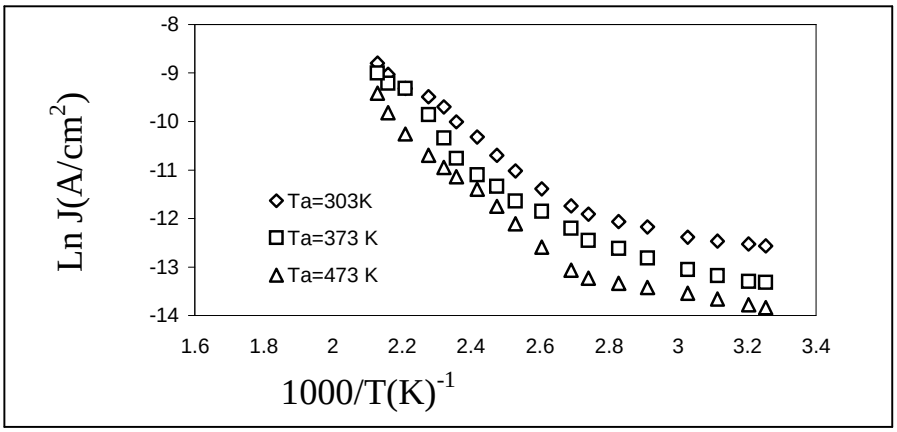


Fig.(3-23)Ln J versus 1000/T for for Al/c-Si/Au for thickness 0.2µm and annealing temperuters

Table (3-3) D.C. conductivity parameter for Al/Si/In ,Al/ Si/Ag and In/Si/Au

	th(μm)	T_a (K)	E_{a1} (eV)	Temperature Rang(K)	E_{a2} (eV)	Temperature Rang(K)
Al/c-Si/In	0.1	٣٠٣	0.046	303- 340	0.24	340-434
		٣٧٣	0.053	303-349	0.28	349-434
		٤٧٣	0.050	303-340	0.29	340-434
	0.2	٣٠٣	0.045	303-362	0.266	362-434
		٣٧٣	0.057	303-348	0.31	348-434
		٤٧٣	0.068	303-362	0.48	362-434
Al/c-Si/Ag	0.1	٣٠٣	0.073	303-382	0.31	382-471
		٣٧٣	0.074	303-382	0.322	382-471
		٤٧٣	0.099	303-392	0.399	392-471
	0.2	٣٠٣	0.076	303-355	0.36	355-471
		٣٧٣	0.079	303-343	0.42	343-471
		٤٧٣	0.11	303-375	0.43	375-471
Al/c-Si/Au	0.2	٣٠٣	0.08	303-343	0.45	343-473
		٣٧٣	0.10	303-343	0.48	343-473
		٤٧٣	0.12	303-352	0.51	352-473

It is clear that the activation energies increasing with increasing of the thickness, may be due to decrease in absorption and increase in energy gap with increase of thickness.

From Table (3-3) we can notice that the activation energies increase with increasing of annealing temperatures as shown in Figures (3-24), (3-25) and (3-26). The main reason is that the activation energies increase with the improvement of the crystal structure and the recrestallization [48].

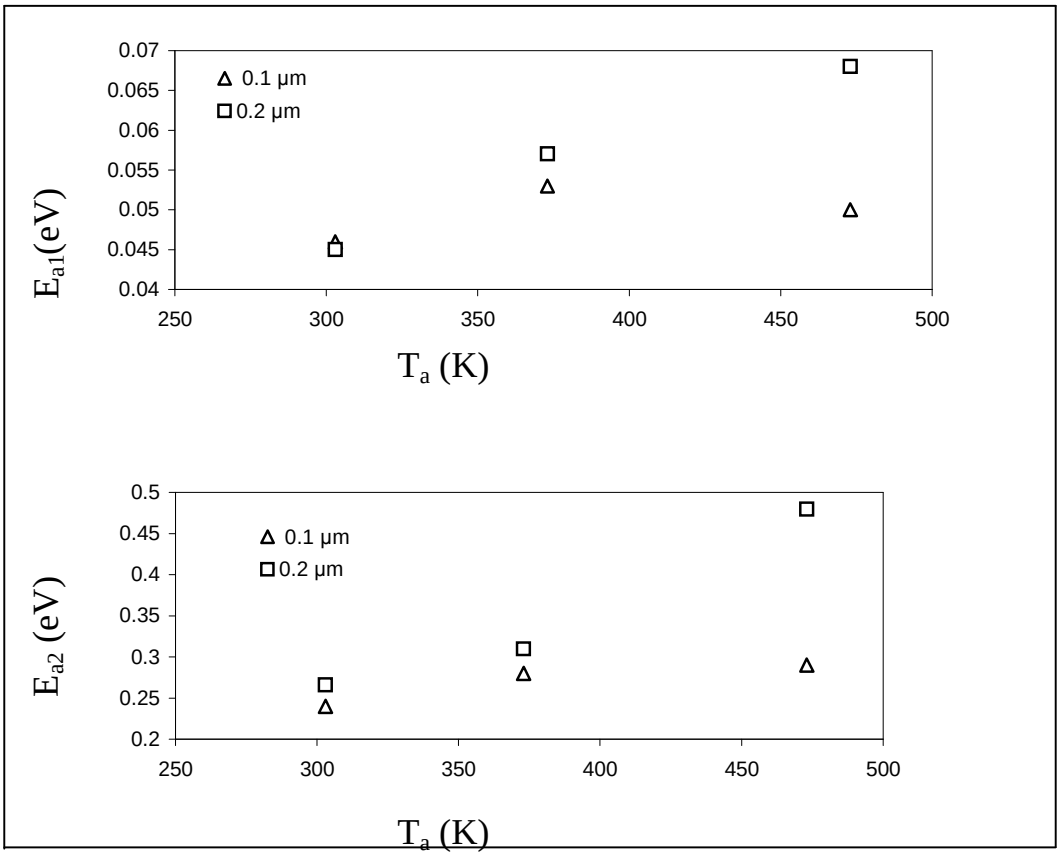


Fig.(3-24)Variation of E_{a1} and E_{a2} for for Al/c-Si/In at different thickness and annealing temperuters

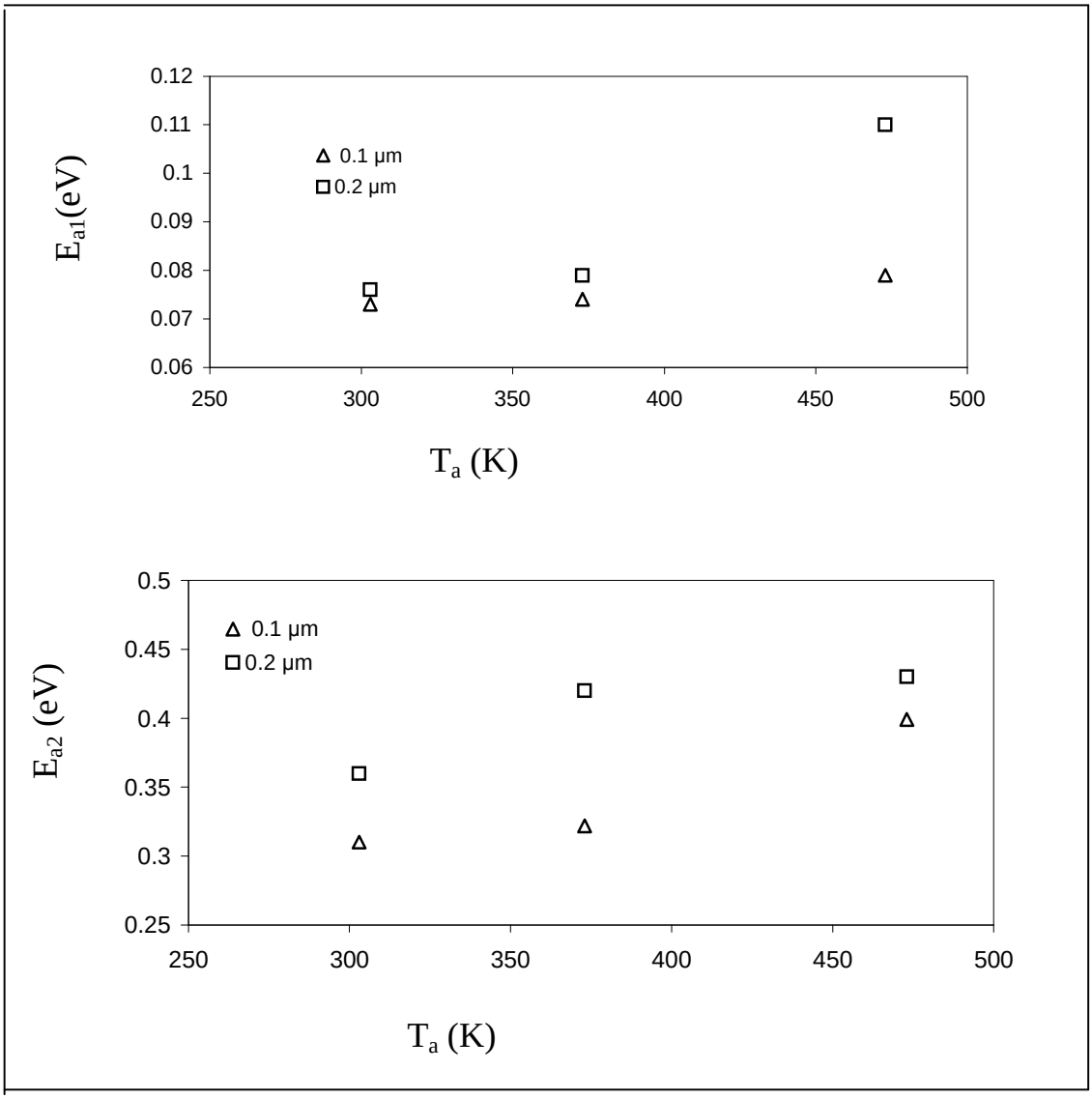


Fig.(3-25) Variation of E_{a1} and E_{a2} for for Al/c-Si/Ag at different thickness and annealing temperuters

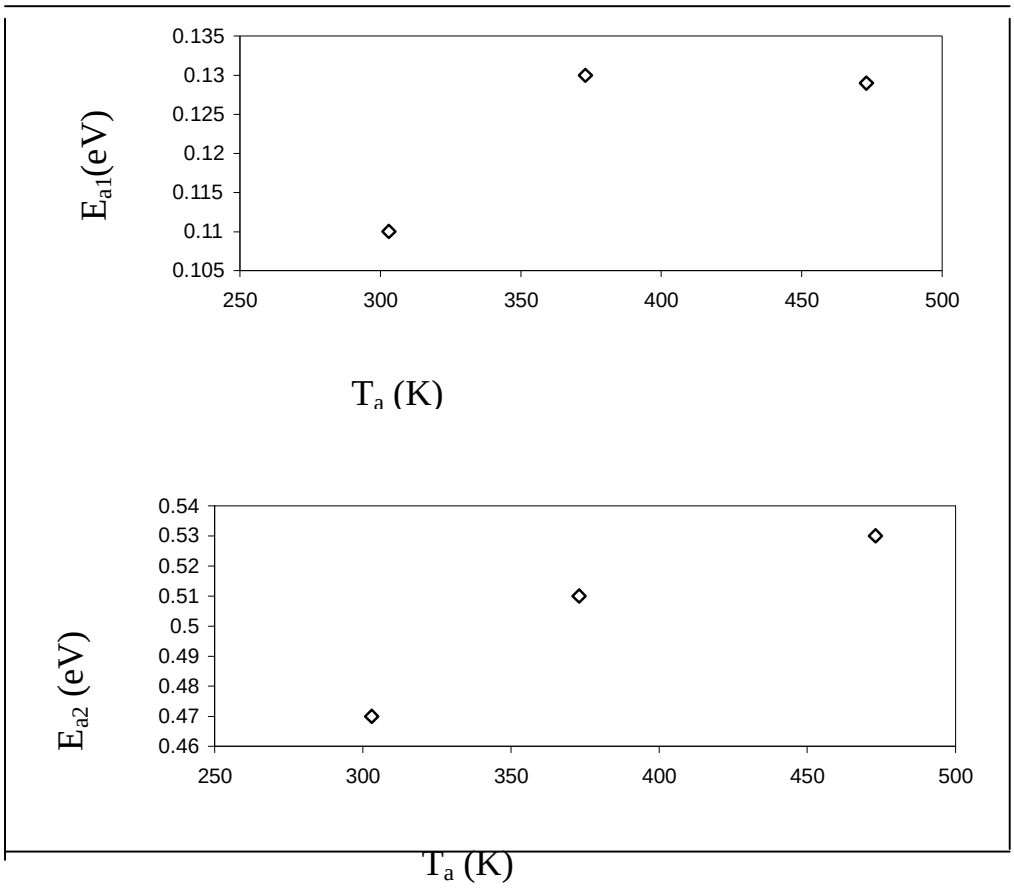


Fig.(3-26)Variation of E_{a1} and E_{a2} for Al/c-Si/Au for thickness 0.2µm and annealing temperatures

Rrr

Fig(4.5) Effect annealing tempertures on ideality factors and saturation current density for Al/Si/Ag

4-5 I-V Characteristic of Al/c-Si/In Schottky Junction Under Illumination

The photocurrent is the current generated by the absorption of photons. It is considered as in important parameter, which acts on the spectral responsivity.

A photovoltaic effect occurs in a material in which there is a space charge layer. When a photo exited electron-hole pair enters the layer, the

electron and hole are separated by the space charge field to give a photo current, the magnitude of the electric field in the space charge region decrease and so the resistivity increases.

The relation between the photocurrent (I_{ph}) and reverse bias voltage (V_R) of the Al/c-Si/In structure at different thickness and annealing temperatures are presented in Figure (4.16-a, b). The measurements were carried out under different incident power density equal to

(0, 32.4,55.5,69,105) mw/cm^2 respectively.

From this Figures we observe that the photocurrent increases with increasing of the bias voltage, i.e. I_{ph} increases with increasing of the depletion region width (w) as shown in the relation below

$$I_{ph} = qaG_{ph}\left(L_p + L_n + W\right) \text{..... (4-1)}$$

Where G_{ph} is the generation rate of photo carriers, L_p and L_n are the diffusion length of holes and electrons respectively.

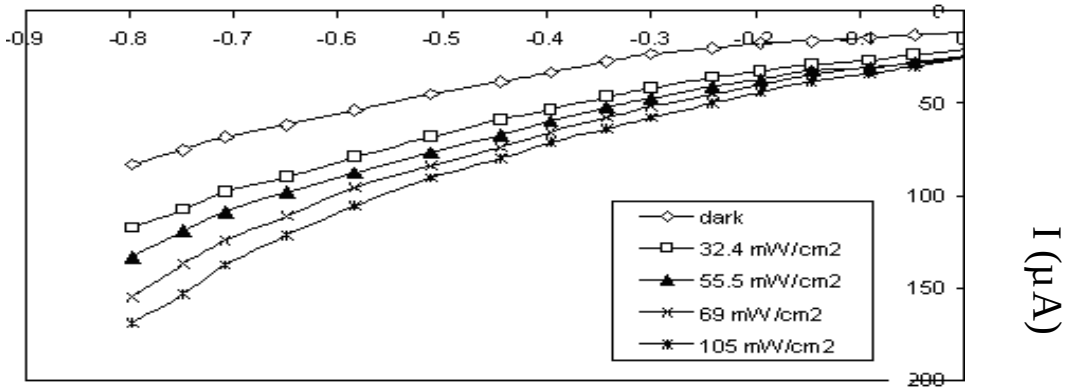
The width of the depletion region increases with increasing of the applied reverse bias voltage. Increasing the reverse bias voltages leads to the increasing in the internal electrical field which leads to an increasing in the probability of the separated electron –hole pairs.

The photocurrent increases with increasing the incident power intensity, due to the increasing in the number of the generated photo carriers in the depletion region with the diffusion depth for carriers which depends on the life time of the minority carriers on the depletion region, this result is in a agreement with results of Sarmah et al [62].

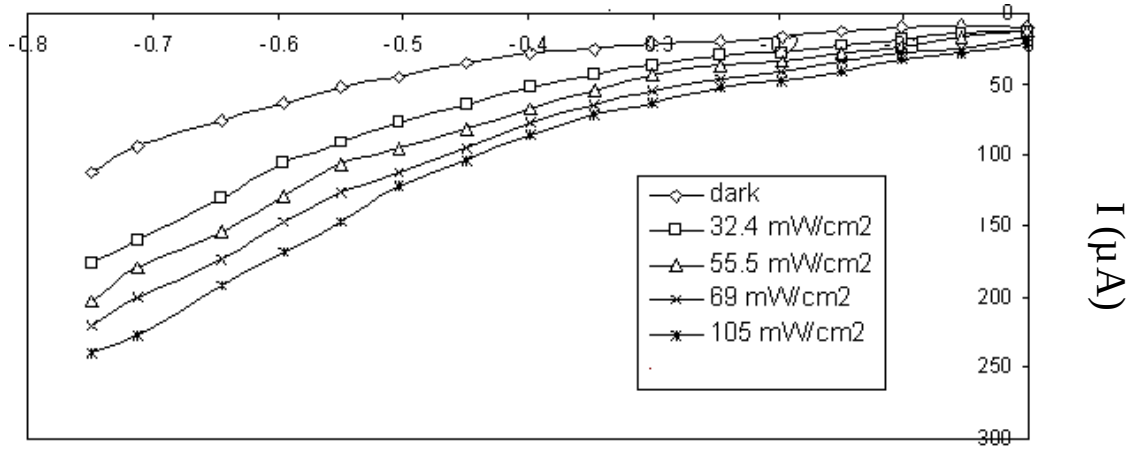
From the same Figures we can see that the photocurrent decreases with increasing of films thickness because the created electron-hole pairs may

recombine before getting separated by the junction and this is attributed to the increase of the structural defects which leads to decrease of the mobility which in turn decreases the current transfer and leads to short diffusion length [62]. We can notice for all samples that the photocurrent increases with increasing of annealing temperature, which is due to the increasing in the grain size and reducing the grain boundaries which lead to the increase of the mobility and increase the photocurrent as well as increase the depletion width which leads to increase of the absorption through it and the creation of electron-hole pairs.

T_a=303 K V(Volt)



T_a=373 K V(Volt)



T_a=473 K

V(Volt)

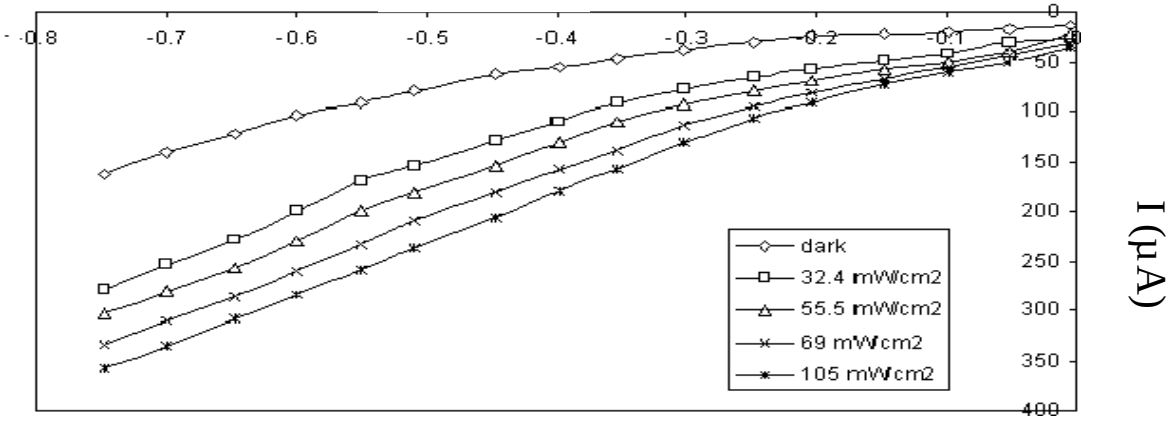


Fig.(4. 16,a) The I-V characteristics under incident power intensity for Al/Si/In at reverse bias at thickness 0.1μm for different annealing temperatures.

V(Volt)

T_a=473 K

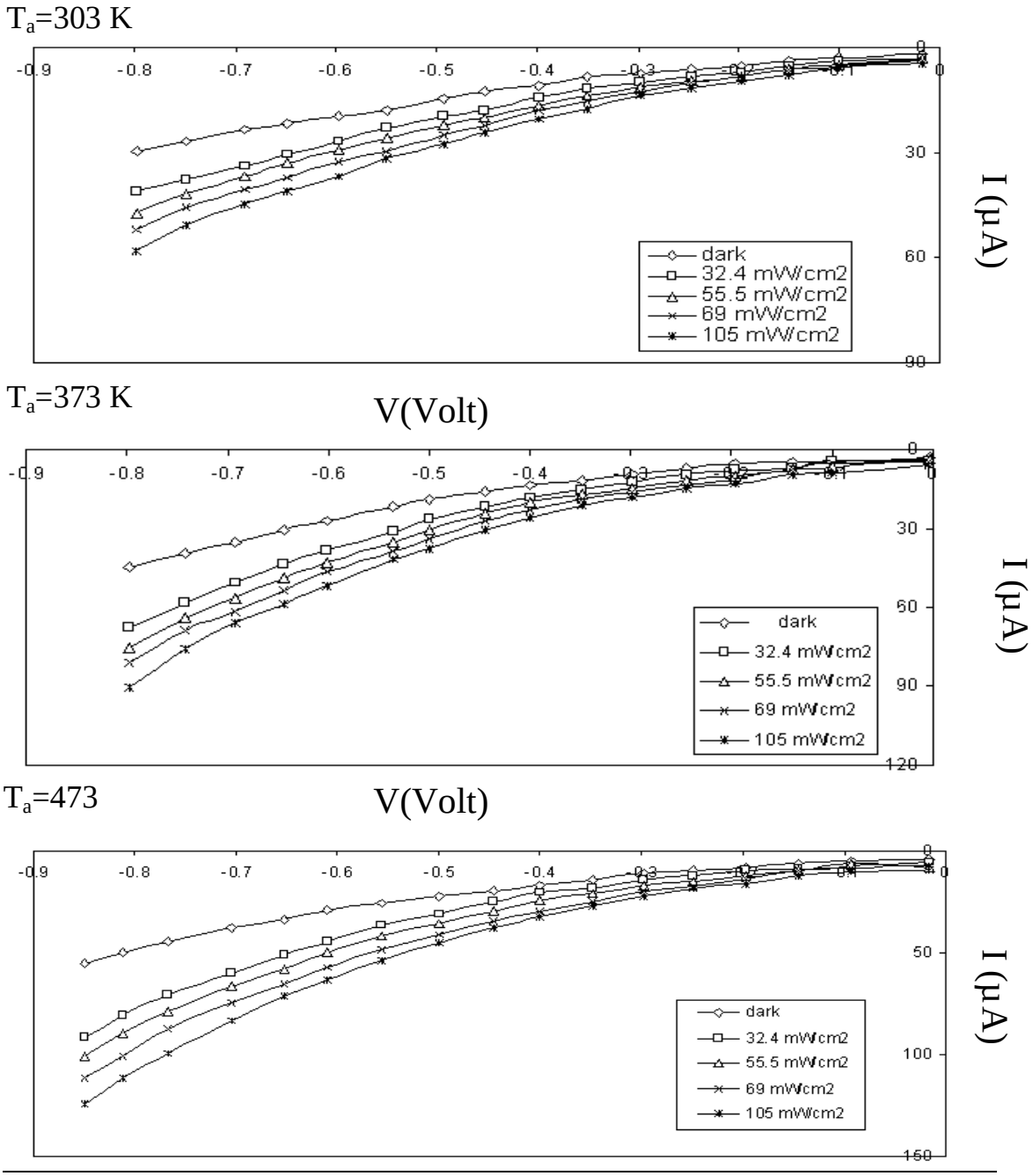


Fig.(Fig.(4.16,b) The I-V characteristics under incident power intensity for Al/Si/In at reverse bias at thickness 0.2μm for different annealing tempertures.

4.4 Capacitance-Voltage characteristics of Al/c-Si/M Schottky diodes

Capacitance versus voltage, referred to as C-V measurement can be used to study the most basic properties of semiconductor junction. In addition to obtaining simple capacitance values at a given bias. The data can be manipulated to yield a number of other parameters such as the built-in potential (V_{bi}), the doping profile and the barrier height. C-V measurements also form the basis of more advanced analysis techniques such as deep level transient spectroscopy [43].

The variation of capacitance as a function of reverse bias voltage in the range of (0-0.8) Volt at frequency equal to 1 MHz has been studied, for Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au for different thickness and annealing temperatures as shown in Figures (4.10), (4-11) and (4-12) in these in Figures we observe that the capacitance of structure is decrease with increasing semiconductor thickness. This result confirm by equation $C=A\varepsilon_s/t$, where A is the active area of the junction and ε_s is the dielectric constant and t thickness of semiconductor layer.

It is clear that the capacitance decreases with increasing of the reverse bias voltage and annealing temperatures, the decreasing was non-linear as shown in Figures (4-10), (4-11) and (4-12). Such behavior is attributed to the increasing in the depletion region width, which leads to increase of the value of built– in voltage. This effect has been studied by Sah and Reddi.[59], Milnes and Feucht.[60] and Ghandhi *et al*.[60] and our results are in agreement with their results.

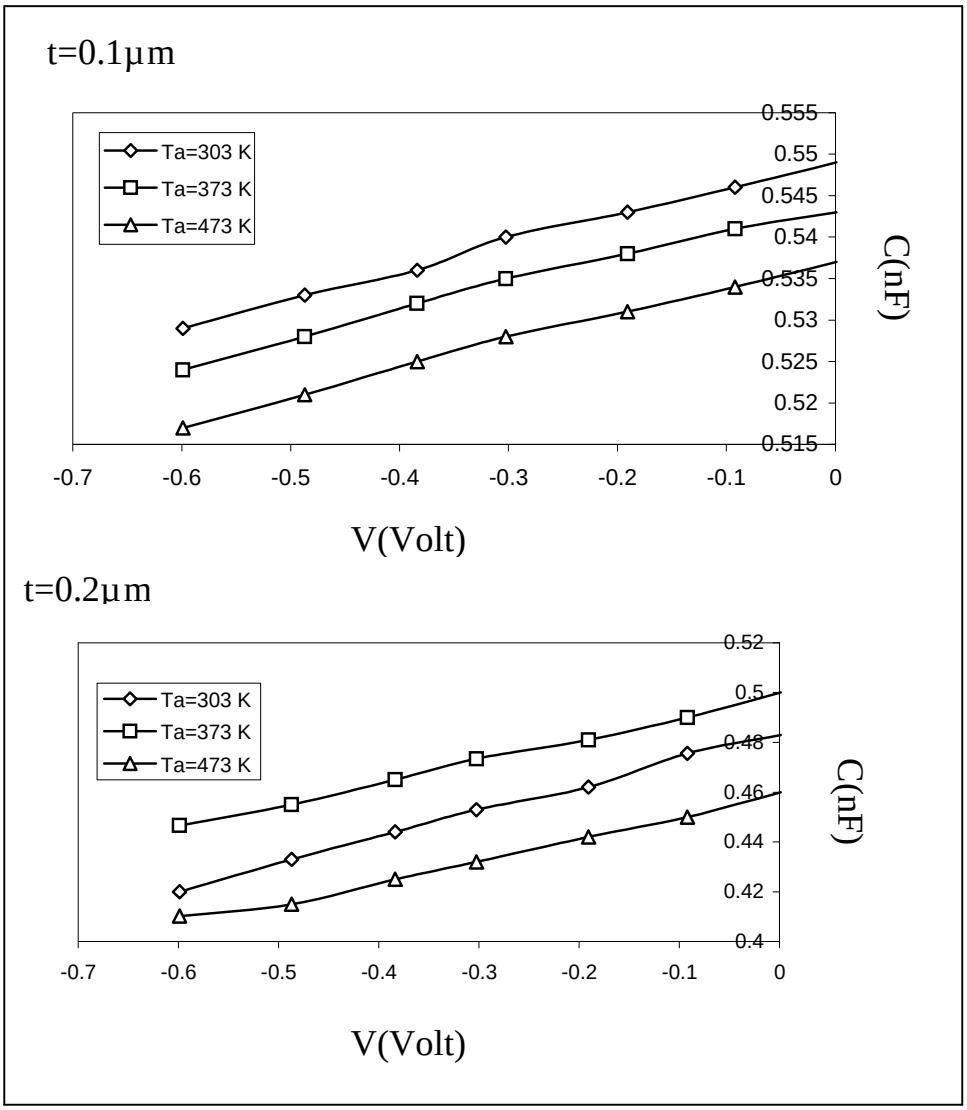


Fig.(4.10) The variation of capacitance as a function of reverse bias voltage for Al/c-Si/In at different thickness and annealing temperatures.

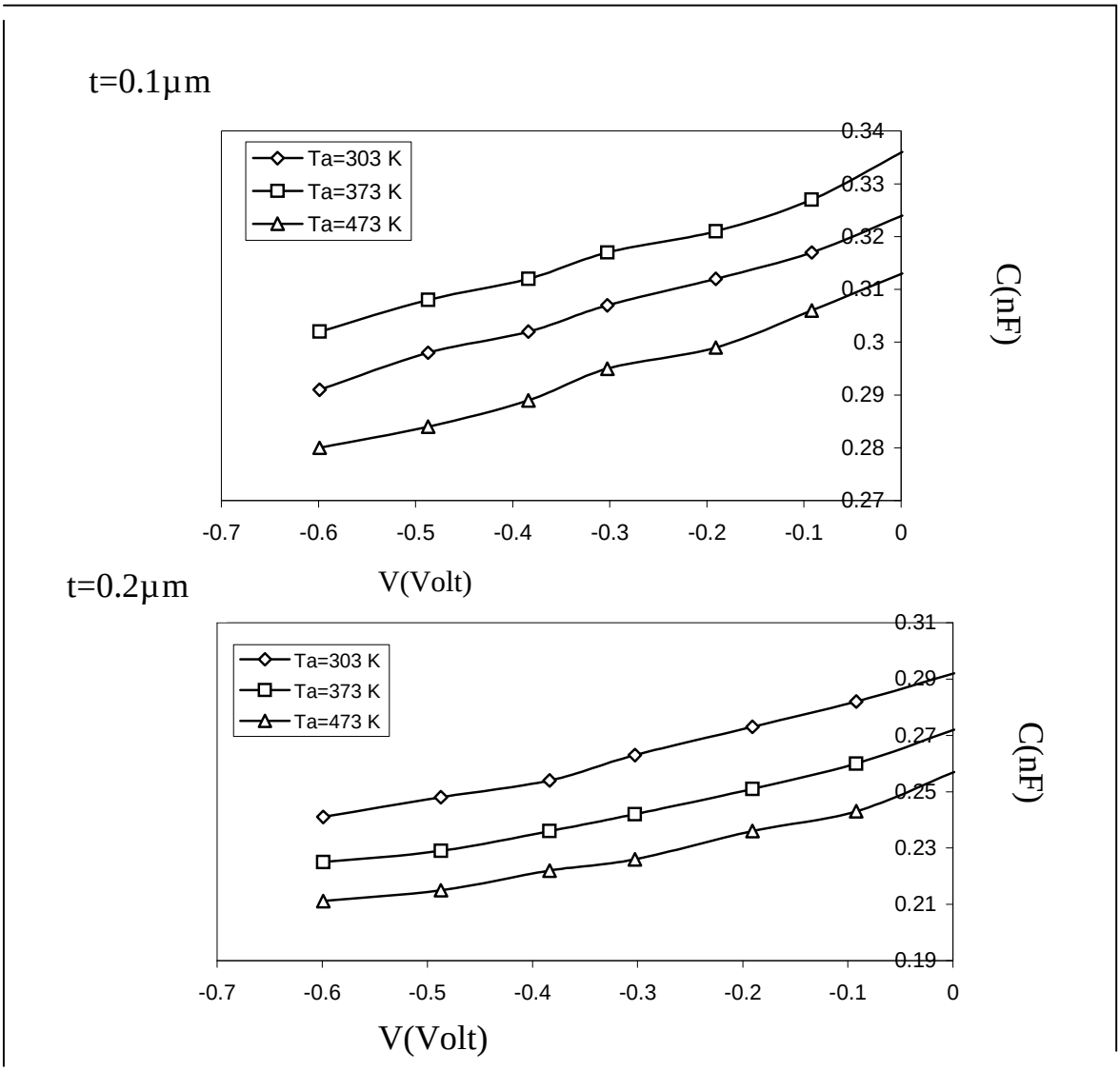


Fig.(4.11) The variation of capacitance as a function of reverse bias voltage for Al/c-Si/Ag at different thickness and annealing temperatures.

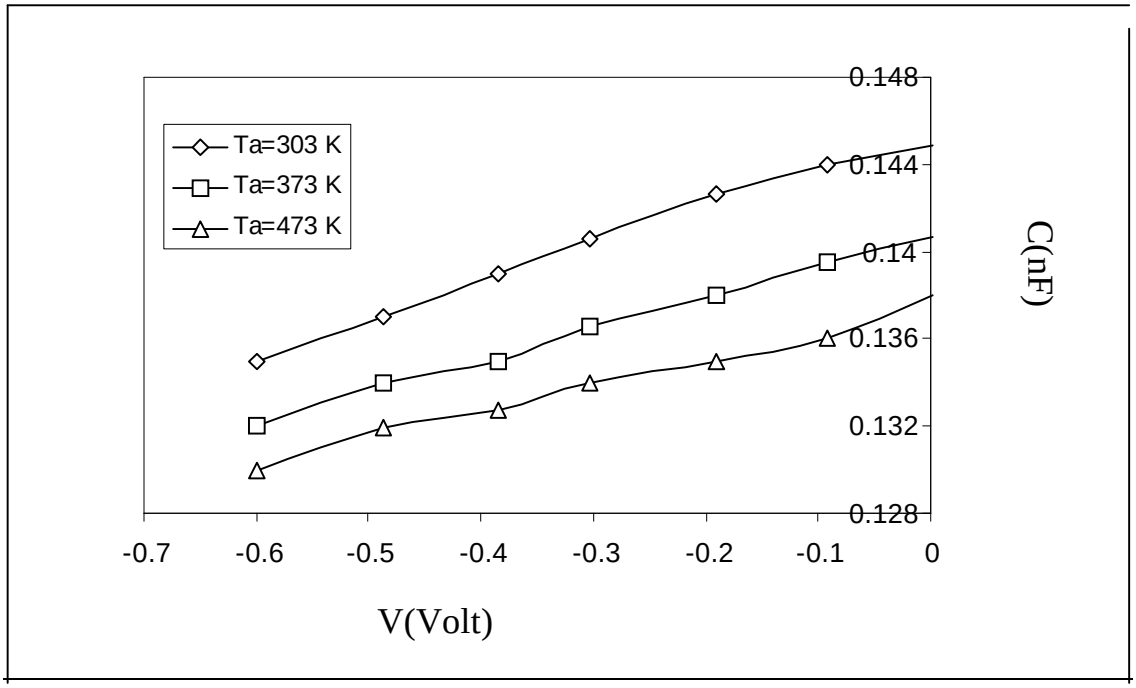


Fig.(4.12) The variation of capacitance as a function of reverse bias voltage for Al/c-Si/Au at 0.2μm and annealing temperatures.

The inverse capacitance square is plotted against applied reverse bias voltage for Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au at different thickness and annealing temperatures as shown in Figures (4.13), (4.14) and (4-15)

A plot of C^{-2} versus V gives a straight line. The linearity in plot of C^{-2} versus V indicates that the charge density within the depletion region of the diode is uniform. This linearity is due to the uniform distribution of the concentration N_a in the band gap. This is in agreement with the results of Ryu and Takashi [61], Nathan and Marinace [62], Jain and Melehy [62] and Milnes and Feucht [63].

The interception of the straight line with the voltage axis at ($1/C^2 = 0$), represents the built in voltage. We observed from Table (4.2) that the built–in voltage increase as a result of the decrease in the capacitance value and the increase of the depletion width.

The slope yields the impurity concentration in the substrates, using equation (3-8). The slope of the curve is inversely proportion to the doping concentration and hence the barrier height (if the shallow level depth is known), using equation (3-9).

The result of built-in voltage, carrier concentration and the barrier height are tabulated in Table (4.2).

We observed from Table (4.2) that the built-in voltage increase with increasing of T_a as a result of the decrease in the capacitance value. Also we can observe that the effect of increasing thickness caused an increase in built-in voltage as given in Table. From the same Figures, we can observe that the effect of increasing thickness caused a increase in built-in voltage as given in Table. From the same Figures, we can notice that the decreasing in the carrier concentration which lead to decrease the capacitance.

We can observe from this Figures and Table (4.2) an increasing ϕ_B(CV) are slightly higher than these of I-V and this can be attributed to barrier height lowering due to image force and contribution of tunneling effect.

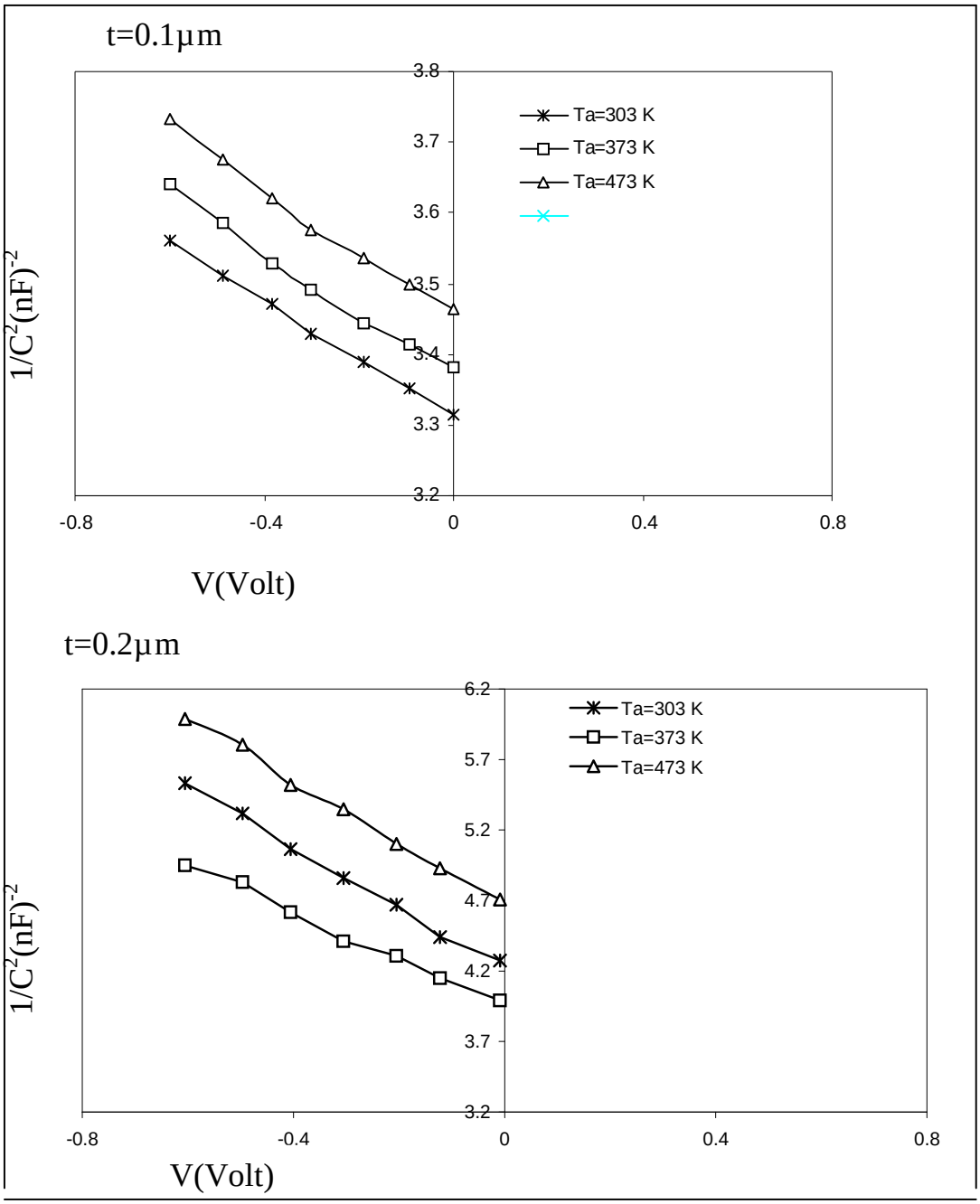


Fig.(4.13) The variation of 1/C2 as a function of reverse bias voltage for Al/c-Si/In at different thickness and annealing temperatures.

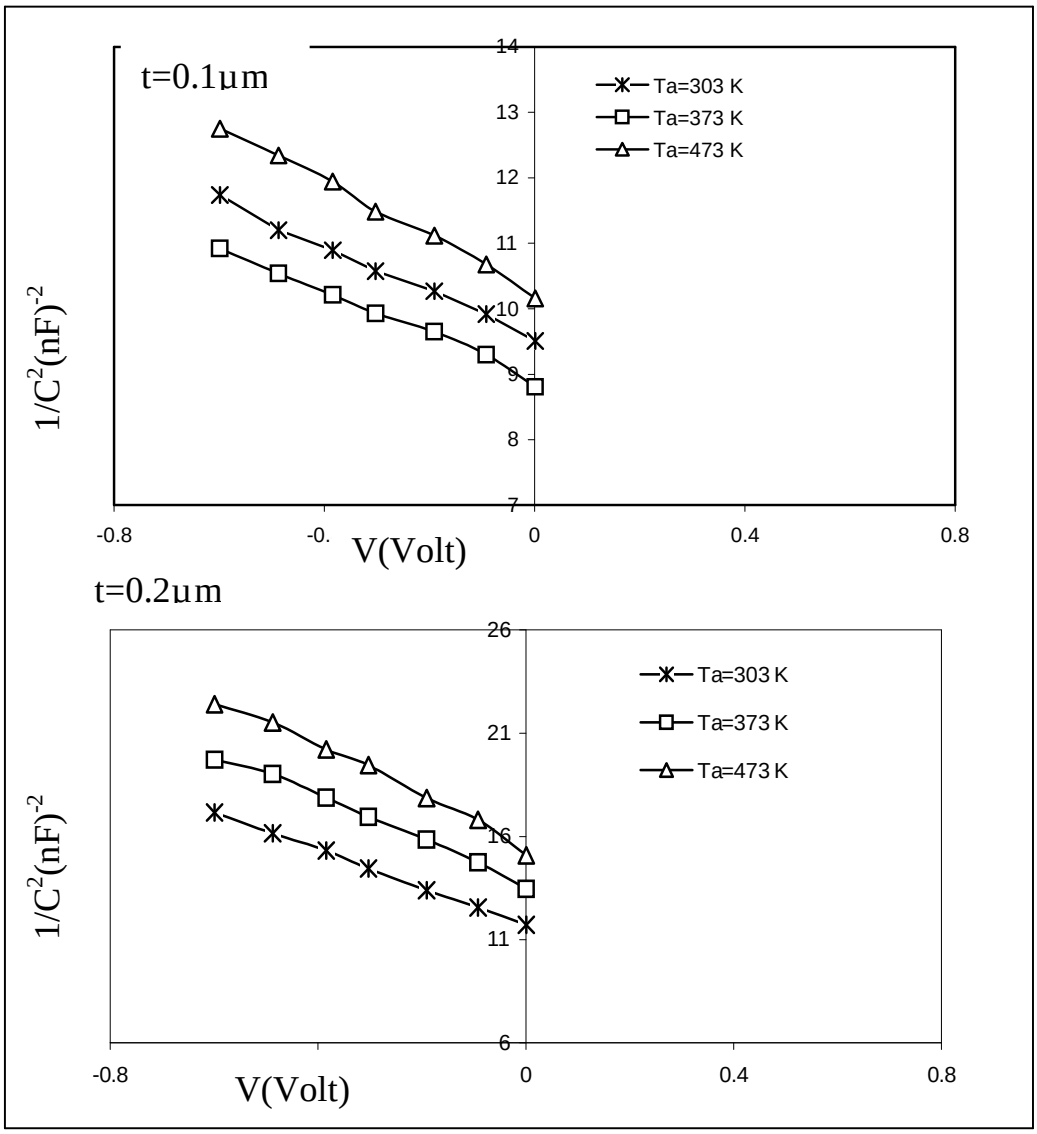


Fig.(4.14) The variation of 1/C2 as a function of reverse bias voltage for Al/c-Si/Ag at different thickness and annealing temperatures

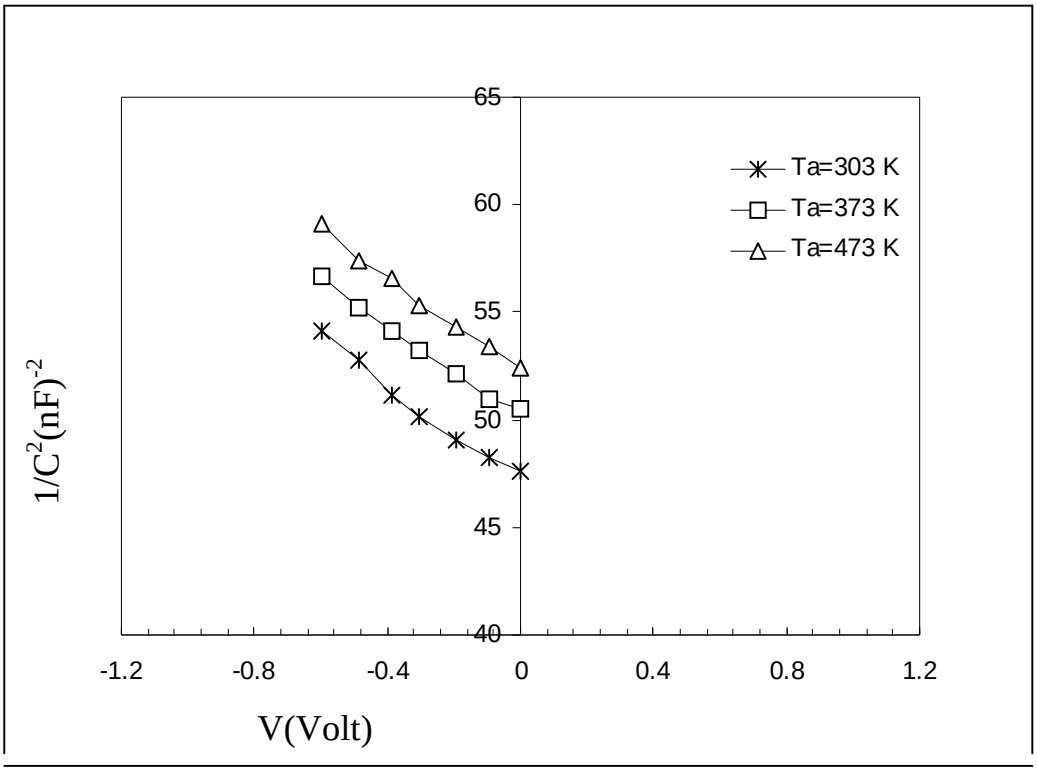


Fig.(4.15) The variation of 1/C2 as a function of reverse bias voltage for Alc-/Si/Au at 0.2µm and annealing temperatures.

Table (4.2) The variation of the N_a , V_{bi} and ϕ_B (C-V) for Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au with different thickness and annealing temperatures.

	t(μm)	T_a (K)	N_a	V_{bi}	$\phi_B(CV)$
Al/c-Si/In	0.1	303	5.79	0.26	0.48
		373	5.48	0.4	0.68
		473	5.34	0.56	0.89
	0.2	303	1.1	0.48	0.65
		373	1.43	0.47	0.79
		473	1.08	0.65	1.09
Al/c-Si/Ag	0.1	303	0.66	0.58	0.84
		373	0.70	0.72	1.06
		473	0.5	0.8	1.27
	0.2	303	0.26	0.59	1.08
		373	0.21	0.67	1.05
		473	0.19	0.78	1.29
Al/c-Si/Au	0.2	303	0.24	0.72	1.1
		373	0.2	0.96	1.16
		473	0.11	1.1	1.21

4.6 D.C. Electrical Conductivity

The variation of electrical current density as a function of temperature at different thickness and annealing temperatures is shown in Figures (4.15), (4.16) and (4.17). Its clear from this Figures that the current density for all deposited films decrease with increase thickness. Also it observed that the current density of the films decrease with increasing of T_a from 303K to 473K.This variation is thought to be due to the changes in crystalline (reduction of the number of grain boundaries due to the increase of grain size).

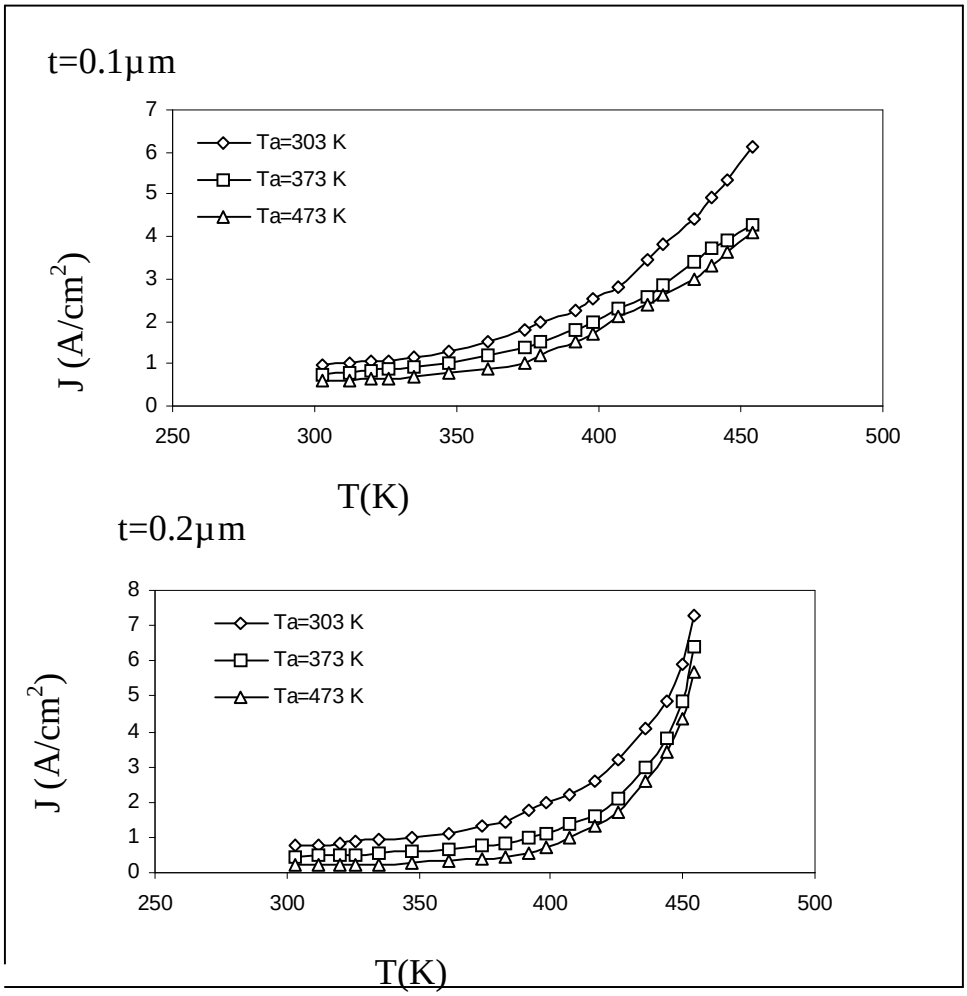


Fig.(4.15) Variation of J D.C versus temperatures for Al/c-Si/In prepared at different thickness and annealing temperatures.

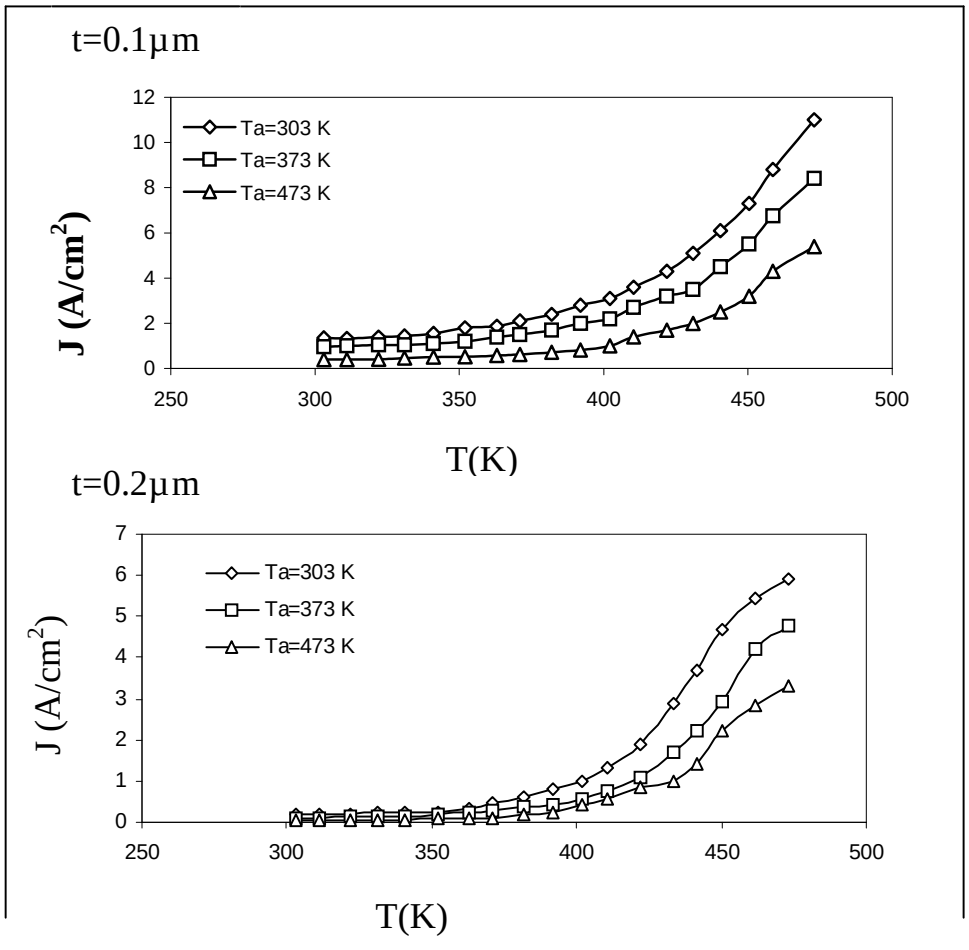


Fig.(4.16) Variation of J D.C versus temperatures for Al/c-Si/Ag prepared at different thickness and annealing temperatures.

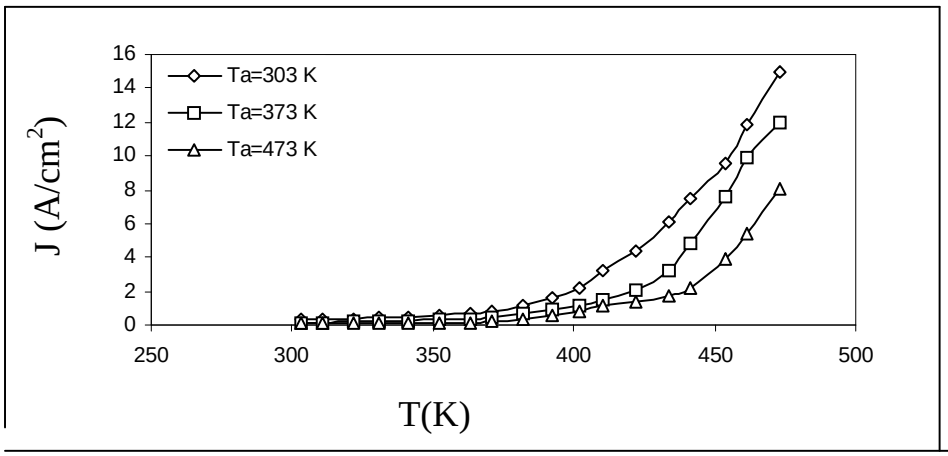


Fig.(4.17)Variation of J D.C versus temperatures Al/c-Si/Au prepared at different thickness and annealing temperatures.

It was plott Ln J versus 1000/T to study the dependence of D.C. conductivity for the as-deposited and annealing samples in the range 303 to 473 at different thickness and annealing temperatures, is shown in Figures (4. 18), (4.19) and (4.20).

It is clear from this Figures that there are two transport mechanisms, giving rise two activation energies E_{a1} and E_{a2} . At the lower range of temperatures, the conduction mechanism is due to carriers excitation into localized state at the edge of the band and at the higher temperatures, the conduction mechanism is due to carriers excitation into the extended states beyond the mobility edge. Similar observation was reported by Valdez[ ].

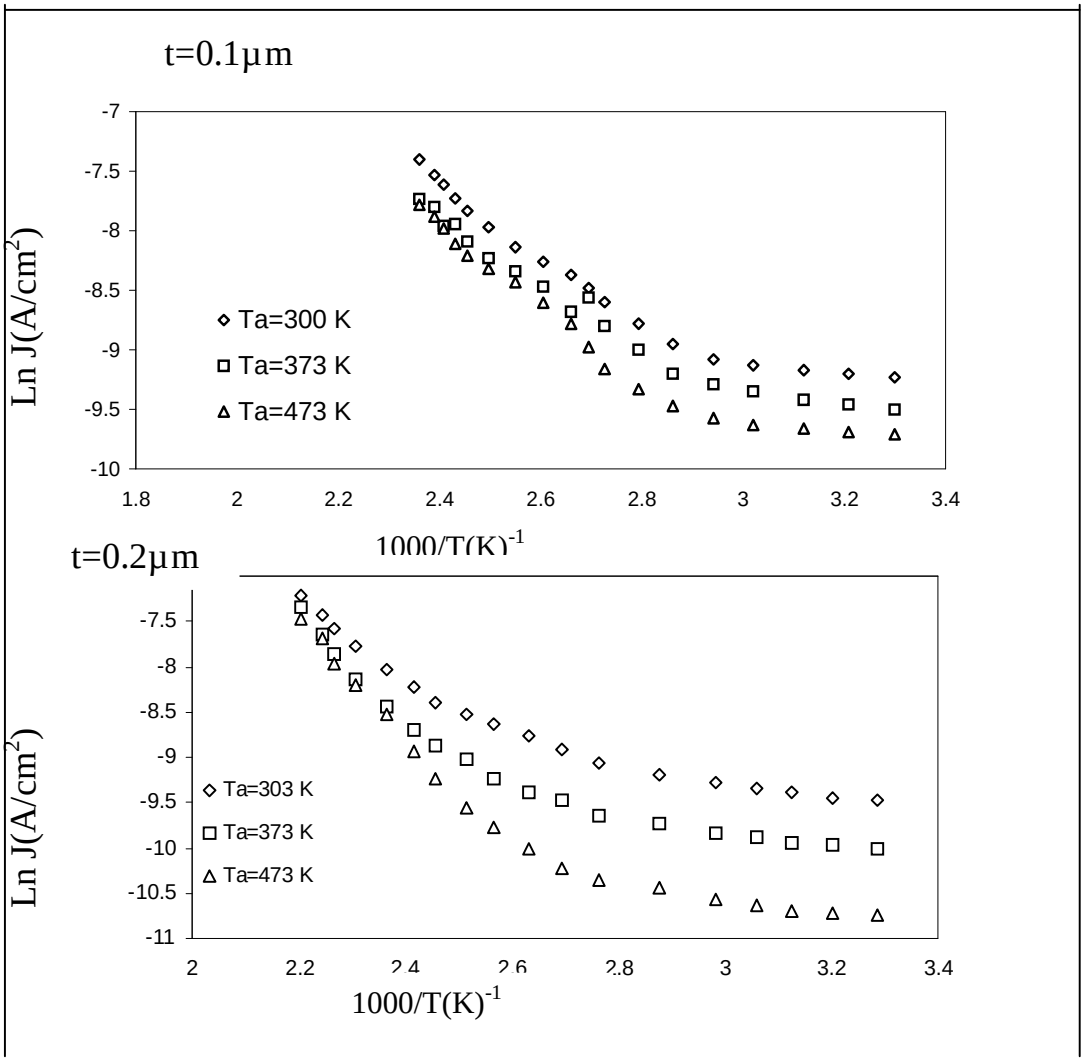


Fig.(4.18) Ln J versus 1000/T for for Al/Si/In at different thickness and annealing temperuters

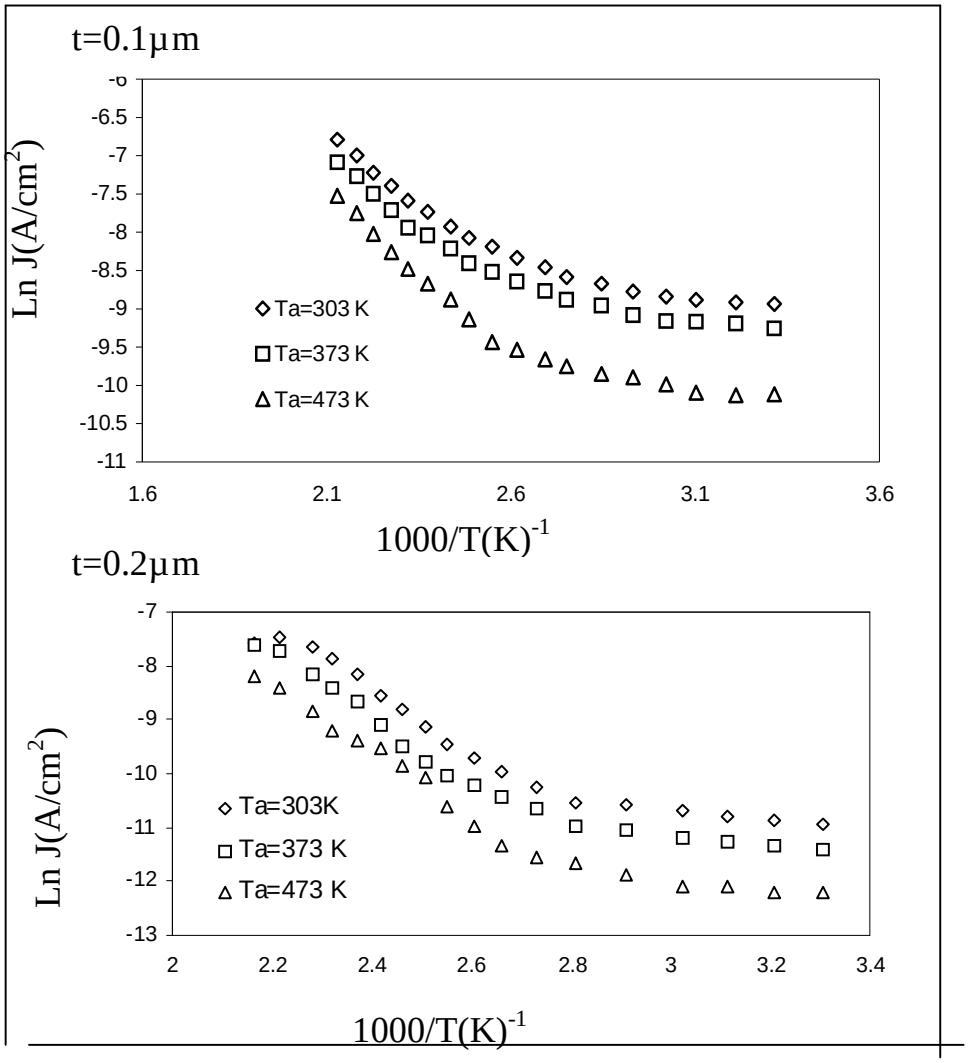


Fig.(4.19) Ln J versus 1000/T for for Al/c-Si/Ag at different thickness and annealing temperuters.

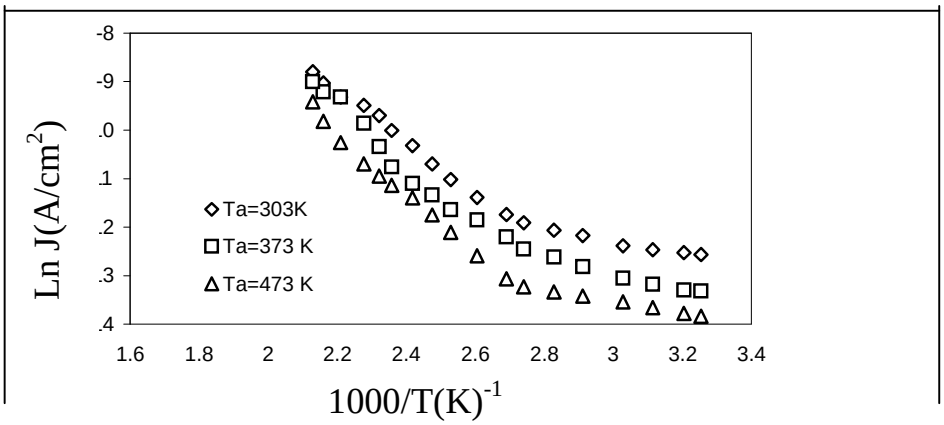


Fig.(4.20) Ln J versus 1000/T for for Al/c-Si/Au for thickness 0.2μm and annealing temperuters

Table (4.3) D.C. conductivity parameter for Al/Si/In ,Al/ Si/Ag and In/Si/Au

	t(µm)	T_a (K)	E_{a1} (eV)	Temp.Rang (K)	E_{a2} (eV)	Temp.Rang (K)
Al/c-Si/In	0.1	300	0.046	303-340	0.24	340-434
		373	0.053	303-349	0.28	349-434
		473	0.050	303-340	0.29	340-434
	0.2	300	0.045	303-362	0.266	362-434
		373	0.057	303-348	0.31	348-434
		473	0.068	303-362	0.48	362-434
Al/c-Si/Ag	0.1	300	0.073	303-382	0.31	382-471
		373	0.074	303-382	0.322	382-471
		473	0.099	303-392	0.399	392-471
	0.2	300	0.076	303-355	0.36	355-471
		373	0.079	303-343	0.42	343-471
		473	0.11	303-375	0.43	375-471
Al/c-Si/Au	0.2	300	0.08	303-343	0.45	343-473
		373	0.10	303-343	0.48	343-473
		473	0.12	303-352	0.51	352-473

It is clear that the activation energyies increasing with inceasing of the thickness , may be due to decrease in absorption and increase in energy gap with increase of thickness.

From Table (4.3) we can notice that the activation energyies increase with increasing of annealing tempertures . The main reason is that the activation energies increase with the improvement of the crystal structure and the recrestallization [60]. This result is in agreement with Islam and Mitra. [62], El-Wahha and Segui et al. [55]

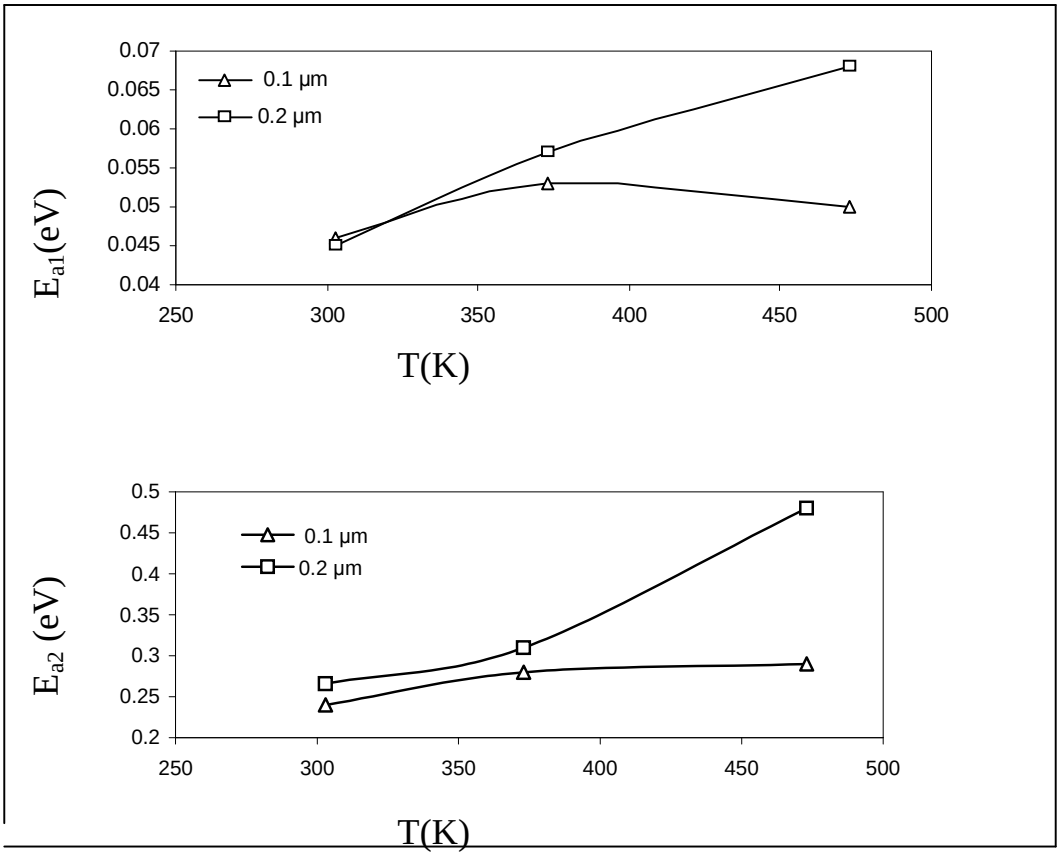


Fig.(4.21) Variation of E_{a1} and E_{a2} for for Al/c-Si/In at different thickness and annealing temperuters

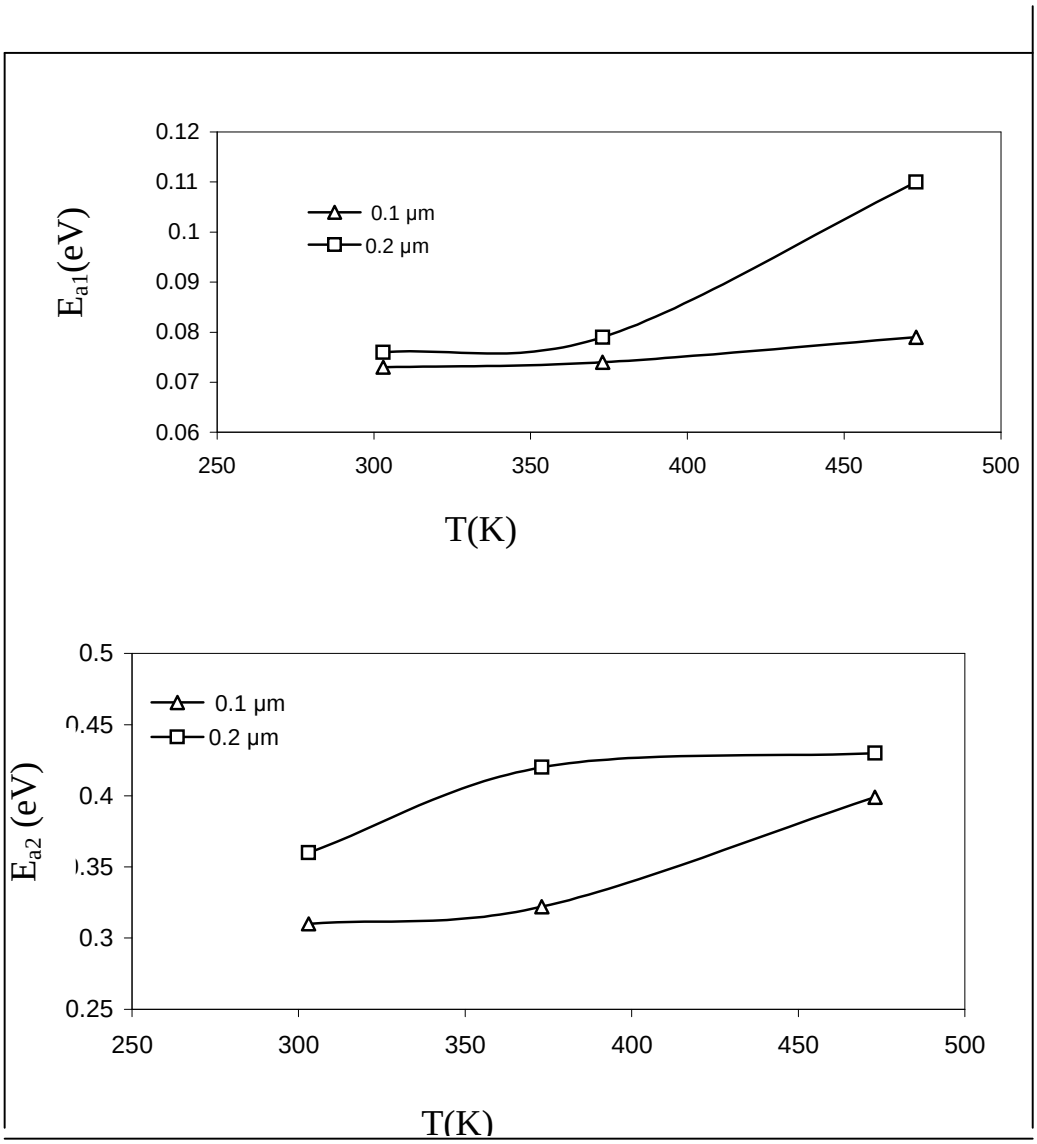


Fig.(4.22) Variation of E_{a1} and E_{a2} for for Al/c-Si/Ag at different thickness and annealing temperuters

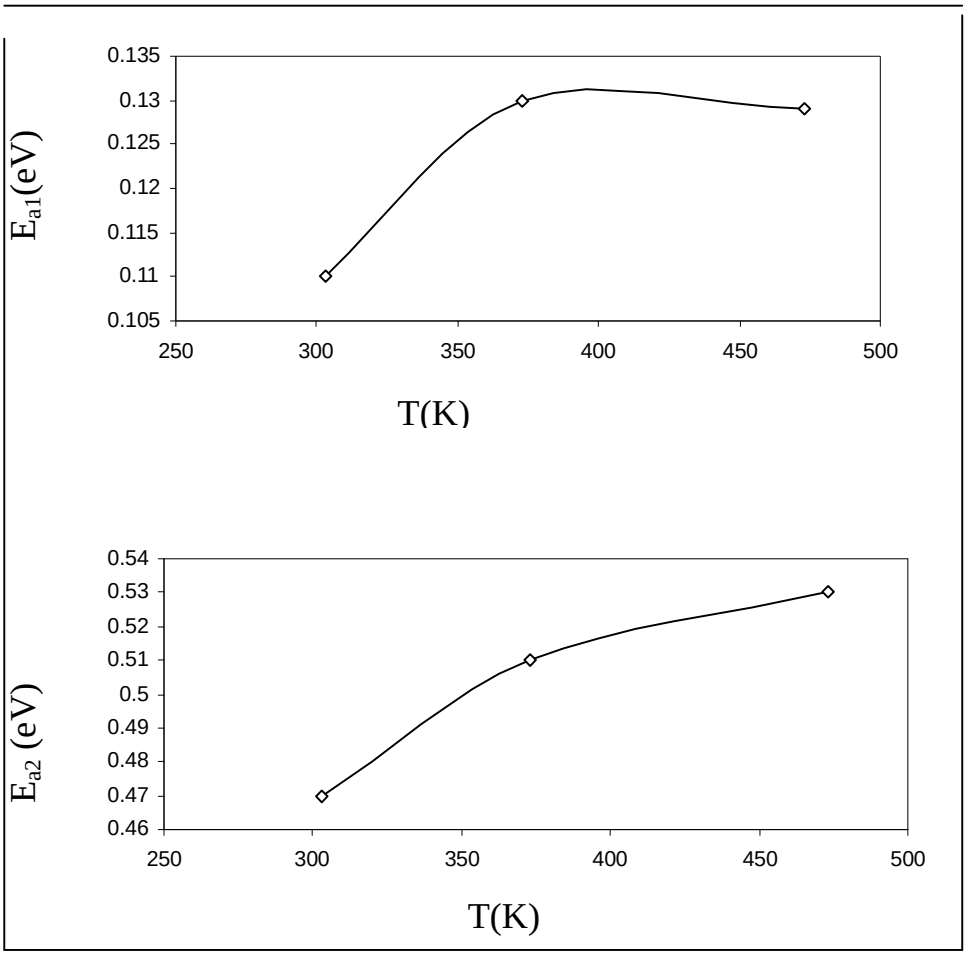


Fig.(4.23) Variation of E_{a1} and E_{a2} for Al/c-Si/Au for thickness 0.2µm and annealing temperatures

Contents

List of Symbols and Abbreviations

Symbol	Description
A	The area of The Junction
A^*	Richardson constant
C	Capacitance
C-V	Capacitance-Voltage
c-Si	Crystalline silicon
E_a	Electrical activation energy
E_F	Fermi level energy
F_x	Image force
G_{ph}	Generation rate of photo carriers
R	Source (boat) to substrate distance.
I	Current
I-V	Current-Voltage
I_{ph}	Photocurrent
I_S	Saturation current
J	Current density
$J_{D.C.}$	D.C. current density.
J_s	Saturation current density
k_B	Boltzman Constant
LED	Light Emitting Diode
L_n	Diffusion Length of Electrons
L_p	Diffusion Length of Holes
m	Mass of the material
M-S	Metal-Semiconductor
n	Ideality Factor
N_a	Acceptors Concentration
N_c	Effective density of states in the conduction band
N_v	Effective density of states in the valence band
ρ_m	Material Density
q = e	Charge of Electron
R_C	Specific Contact Resistance
SBH	Schottky Barrier Height
th	Film Thickness
T	Absolute temperture
T_a	Annealing temperature
V	Applied voltage.
V_{bi}	Built-in Potential

V_F	Forward Voltage
V_R	Reverse Voltage
V_n	The Depth of The Fermi Level Below The Conduction Band
X	Distance between interference frings
ΔX	Shift between interference fringes
ε_s	Static Dielectric Constant of semiconductor
ϕ_B	Barrier Height
ϕ_{Bn}	Barrier Height of n-Type Semiconductor
ϕ_{Bp}	Barrier Height of p-Type Semiconductor
χ_s	Semiconductor Work Function
λ	Wavelength

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$J_{D.C.}$	D.C. current density.
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ϕ_{Bn}	Barrier Height of n-Type Semiconductor
ϕ_{Bp}	Barrier Height of p-Type Semiconductor
χ_s	Semiconductor Work Function
λ	Wavelength

Table (4-2) The variation of the N_a, V_{bi} and $\phi_B(CV)$ for Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au with different thickness and annealing temperatures.

	th (μm)	T_a (K)	N_a(cm^{-3})	V_{bi}(Volt)	$\phi_B(CV)$(eV)
Al/c-Si/In	0.1	٣٠٣	5.79	0.26	0.48
		٣٧٣	5.43	0.4	0.68
		٤٧٣	5.34	0.56	0.89
	0.2	٣٠٣	1.1	0.48	0.65
		٣٧٣	1.43	0.47	0.79
		٤٧٣	1.08	0.65	1.09

Alc-/Si/Ag	0.1	٣٠٣	0.66	0.58	0.84
		٣٧٣	0.70	0.72	1.06
		٤٧٣	0.5	0.8	1.27
	0.2	٣٠٣	0.26	0.59	1.08
		٣٧٣	0.21	0.67	1.05
		٤٧٣	0.19	0.78	1.29
Al/c-Si/Au	0.2	٣٠٣	0.24	0.72	1.1
		٣٧٣	0.2	0.96	1.16
		٤٧٣	0.11	1.1	1.21

Table (4-3) D.C. conductivity parameter for Al/c-Si/In, Al/c-Si/Ag and Al/c-Si/Au

	Thickness(μm)	T_a (K)	E_{a1} (eV)	Temperature Rang(K)	E_{a1} (eV)	Temperature Rang(K)
Al/c-Si/In	0.1	٣٠٣	0.046	303- 340	0.24	340-434
		٣٧٣	0.053	303-349	0.28	349-434
		٤٧٣	0.050	303-340	0.29	340-434
	0.2	٣٠٣	0.045	303-362	0.266	362-434
		٣٧٣	0.057	303-348	0.31	348-434

		٤٧٣	0.068	303-362	0.48	362-434
Al/c-Si/Ag	0.1	٣٠٣	0.073	303-382	0.31	382-471
		٣٧٣	0.074	303-382	0.322	382-471
		٤٧٣	0.099	303-392	0.399	392-471
	0.2	٣٠٣	0.076	303-355	0.36	355-471
		٣٧٣	0.079	303-343	0.42	343-471
		٤٧٣	0.11	303-375	0.43	375-471
Al/c-Si/Au	0.2	٣٠٣	0.08	303-343	0.45	343-473
		٣٧٣	0.10	303-343	0.48	343-473
		٤٧٣	0.12	303-352	0.51	352-473

CERTIFICATION

We certify that this thesis entitled "**Electronic Transport mechanism of Al/c-Si/M Schottky Diodes**" was prepared by "**Russl Abdul Sada Azoz**" under our supervision at College of Science, Al-Nahrain University as a partial fulfillment of the requirements for the degree of **Master of Science in Physics**.

Signature:

Name: **Dr. Hussein. Kh. Rashed**

Title: **Assistant Professor**

Date: **/ / 2008**

Signature:

Name: **Dr. Talib.S. Hamadi**

Title: **Lecturer**

Date: **/ / 2008**

In view of the available recommendations, I forward this thesis for debate by the examination committee.

Signature:

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Title : **Assistant Professor**

Address: **Head of Department of Physics**

Date: **/ /2008**

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Russl

Republic of Iraq
Ministry of Higher Education
and Scientific Research
Al-Nahrain University
College of Science

Electronic Transport Mechanism of Al/c-Si/M Schottky Diodes

A Thesis
Submitted to the College of Science of Al-Nahrain University as a Partial Fulfillment of the Requirements for the Degree of Master of Science in Physics

By

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(B.Sc. 2005)

Supervised by

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٢٠٠٨

جمهورية العراق

وزارة التعليم العالي والبحث العلمي

جامعة النهرين

كلية العلوم

ميكانيكية الانتقال الالكترونيه لثنائي شوتكي

Al/c-Si/M

رسالة

مقدمه الى كلية العلوم جامعة النهرين كجزء من متطلبات الحصول على درجة ماجستير علوم في الفيزياء

من قبل

رسل عبد السادة عزوزعبود

بكالوريوس (٢٠٠٥)

بأشراف

الاستاذ المساعد الدكتور حسين خزعل رشيد

المدرس الدكتور طالب سلوم حمادي

٢٠٠٨

Dedication

To my first and dearest teacher my father

To my mother whose love is plasnted in my Heart

To those whom I love my Brothers And my Sisters

With my best gratitude

Russl

بسم الله الرحمن الرحيم

اقْرَأْ بِاسْمِ رَبِّكَ الَّذِي خَلَقَ ۝ خَلَقَ ألانسَانَ مِنْ عَلَقٍ ۝ اقْرَأْ وَرَبُّكَ الأَكْرَمُ ۝ الَّذِي عَلَّمَ بِالْقَلَمِ ۝ عَلَّمَ الإِنسَانَ مَا لَمْ يَعْلَمْ ۝

صدق الله العظيم

سورة العلق: الايات[1- 5]

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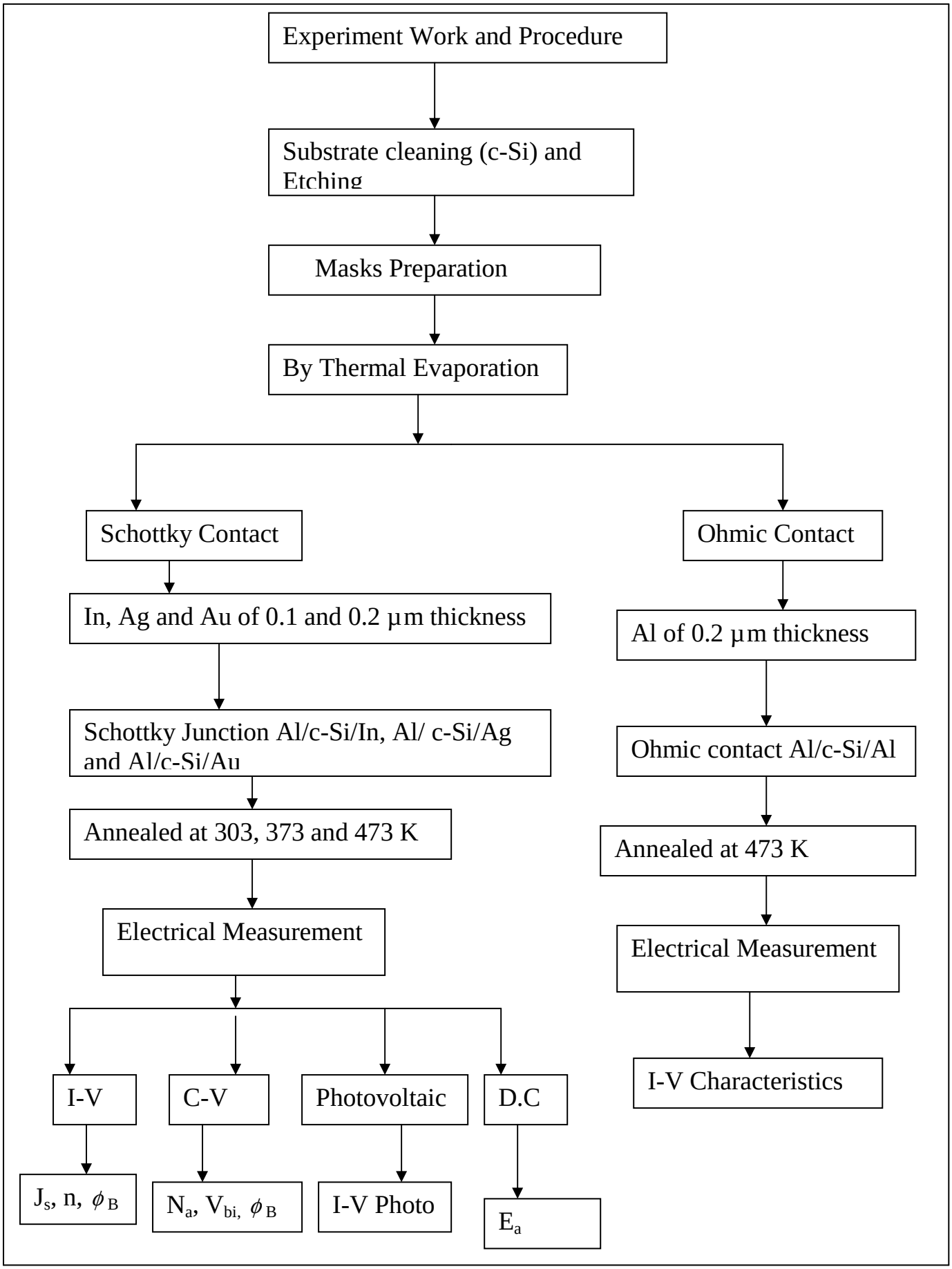


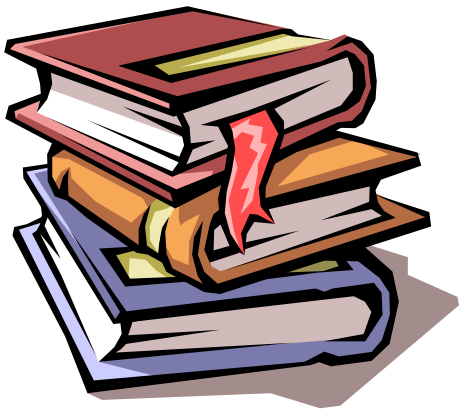
Fig (2-1) The Schematize of the experimental work

Chapter Two

Metal-Semiconductors Contacts

Chapter One

General Introduction

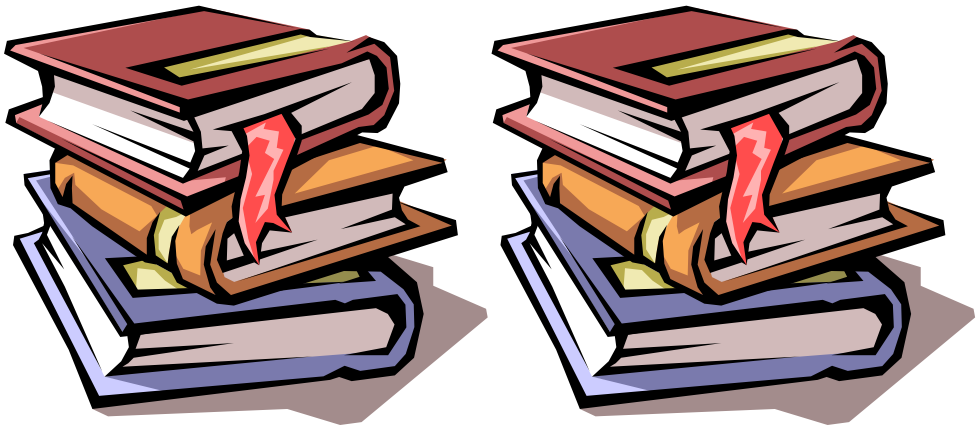


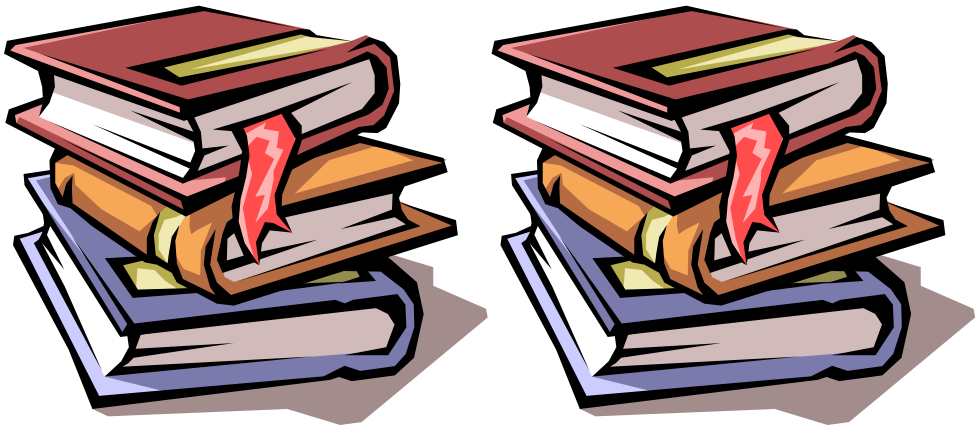
Chapter Three

Experimental Work

Chapter four

Results and Discussion





Chapter Five

Conclusions and Suggestion for Future Work


References